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ATX:226*185

Ver: 10

Intel -KabyLake-S plamform

CPU:

LGA1151

CPU POWER PAK *3 Phase

GT POWER PAK *2 Phase

System Chipset:

Kaby Lake B250

Onboard Chip:

HD Audio Codec: ALC887

SIO: NCT5565D

Flash ROM: SPI 64 MB

DP to VGA: ITE6516

CLR_COMS:SLG4B41231

PWM:

VCORE - RT3606

DDR - RT8231

DDR VPP25- MP2143

PCH(1.0V) - RT8125E

VCCSA - RT8125E

VCCIO - MP5077(Load Switch)

Main Memory:

DDR4 * 2 (Dual Channel)

ACPI:

5VDAUL:uP7501

VCCSTPLL - NMOS

5VDIMM:uP7501

3VSB:GS7133

3VDSW:GS7116

Expansion Slots:

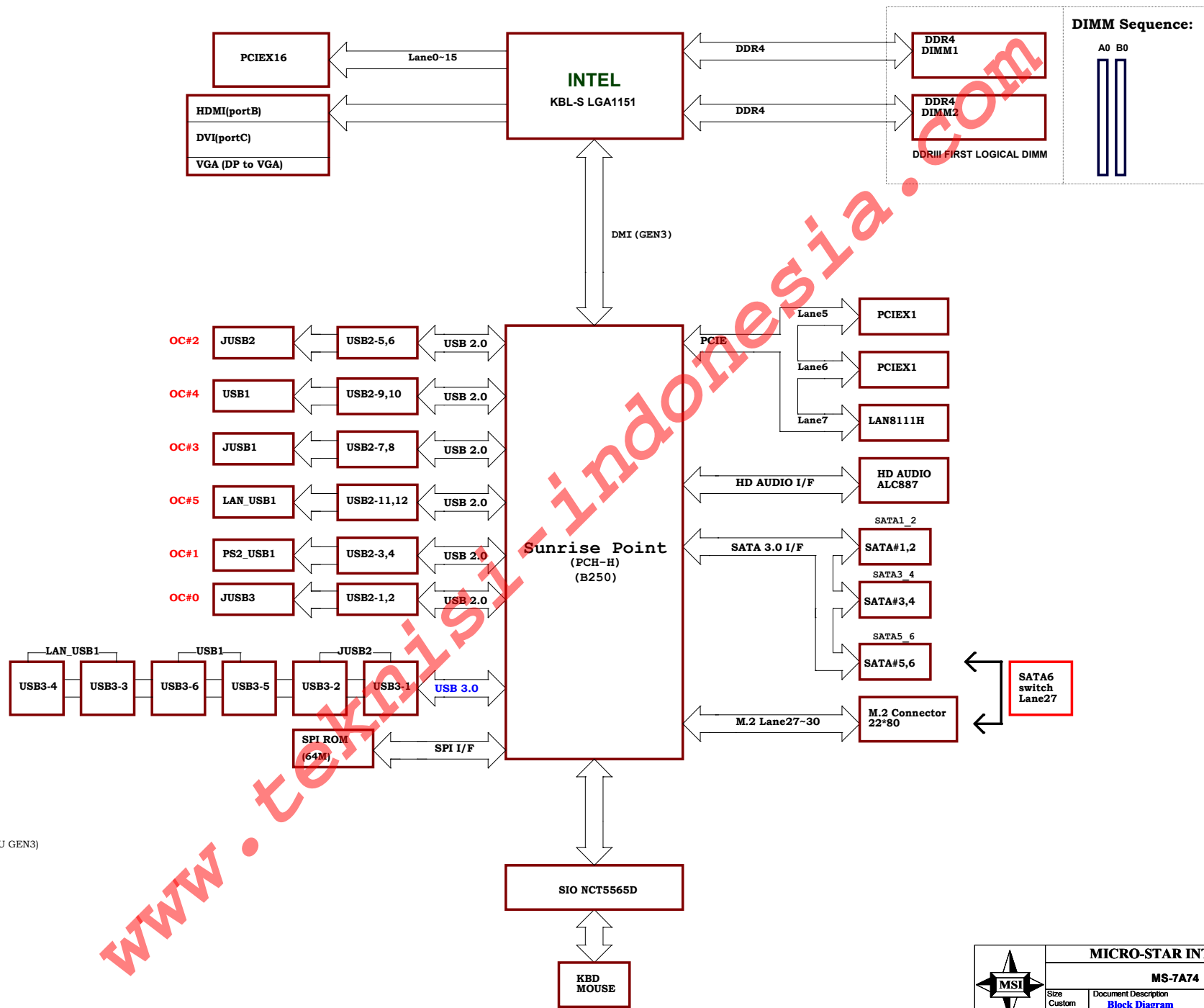
PCI Express (X16) Slot * 1

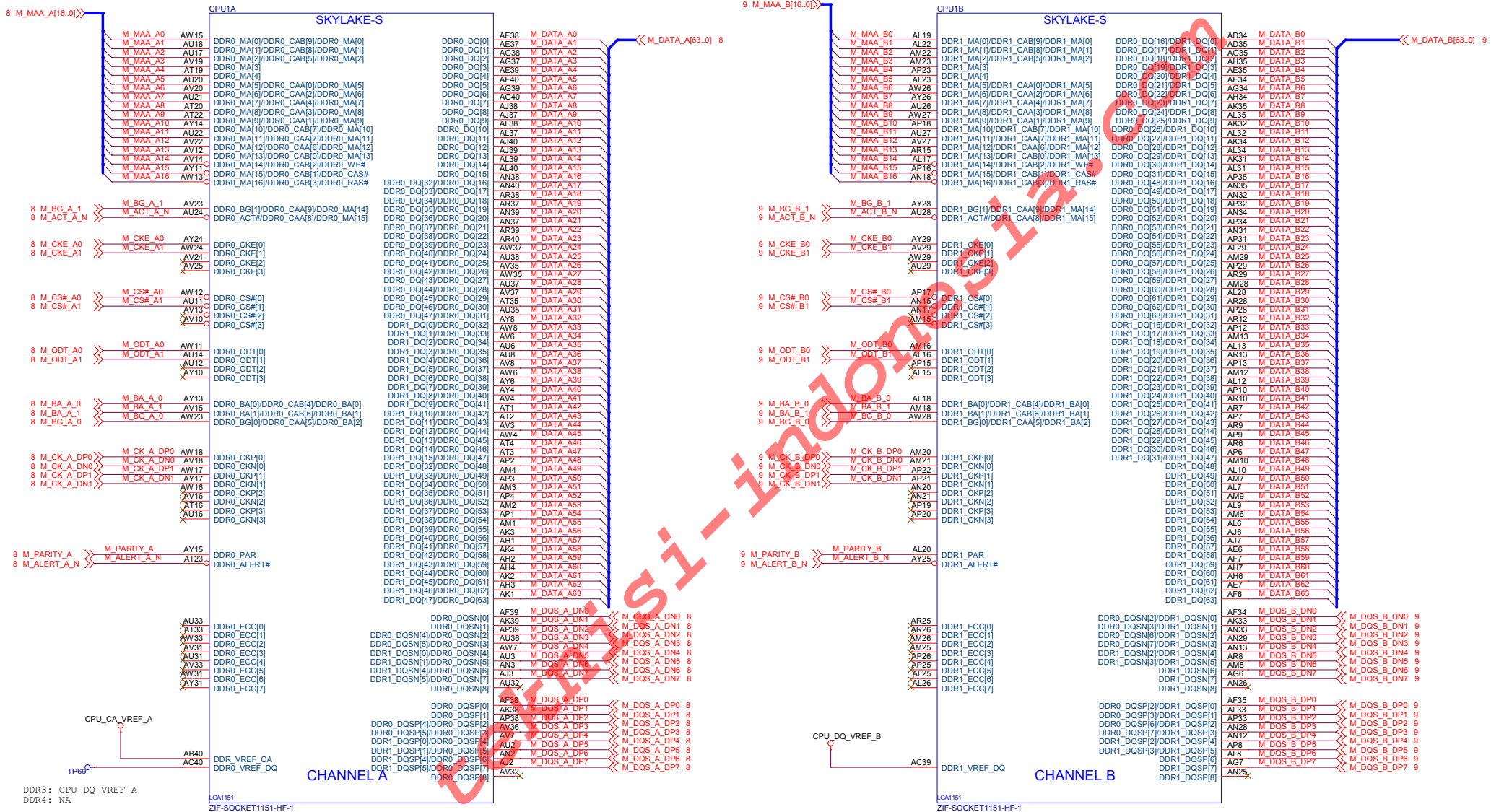
PCI Express (X1) Slot * 2

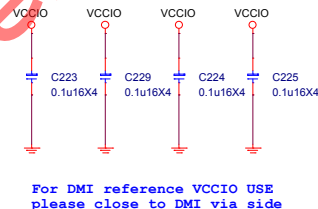
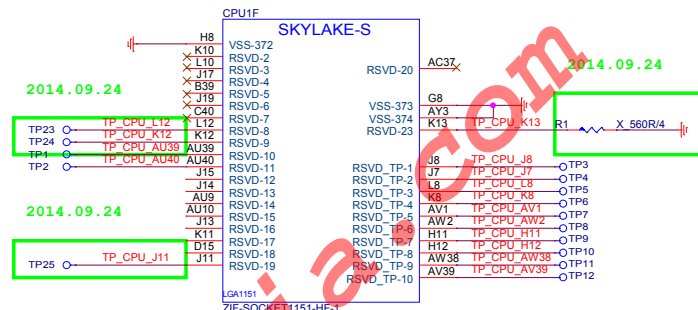
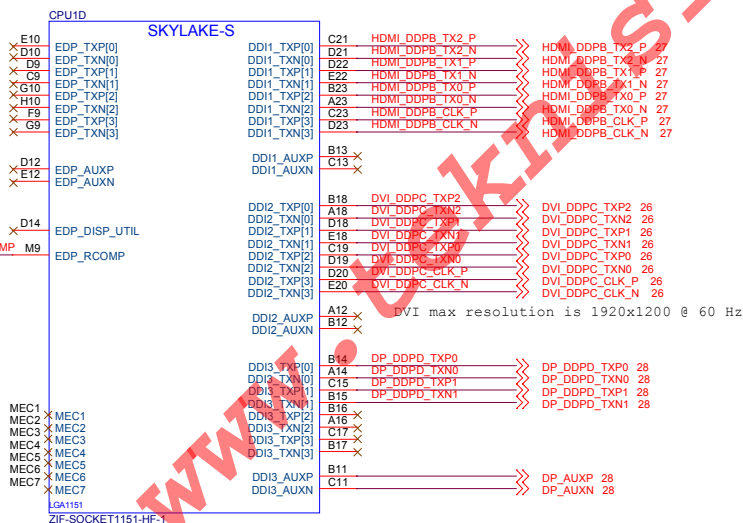
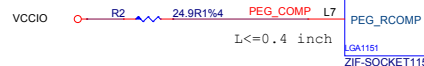
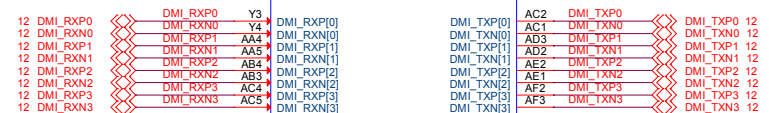
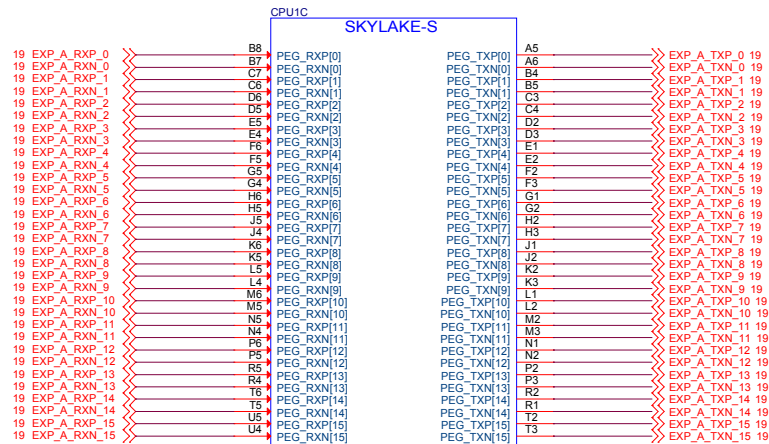
M.2 Slot * 1

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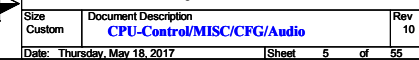
MS-7A74 Block Diagram

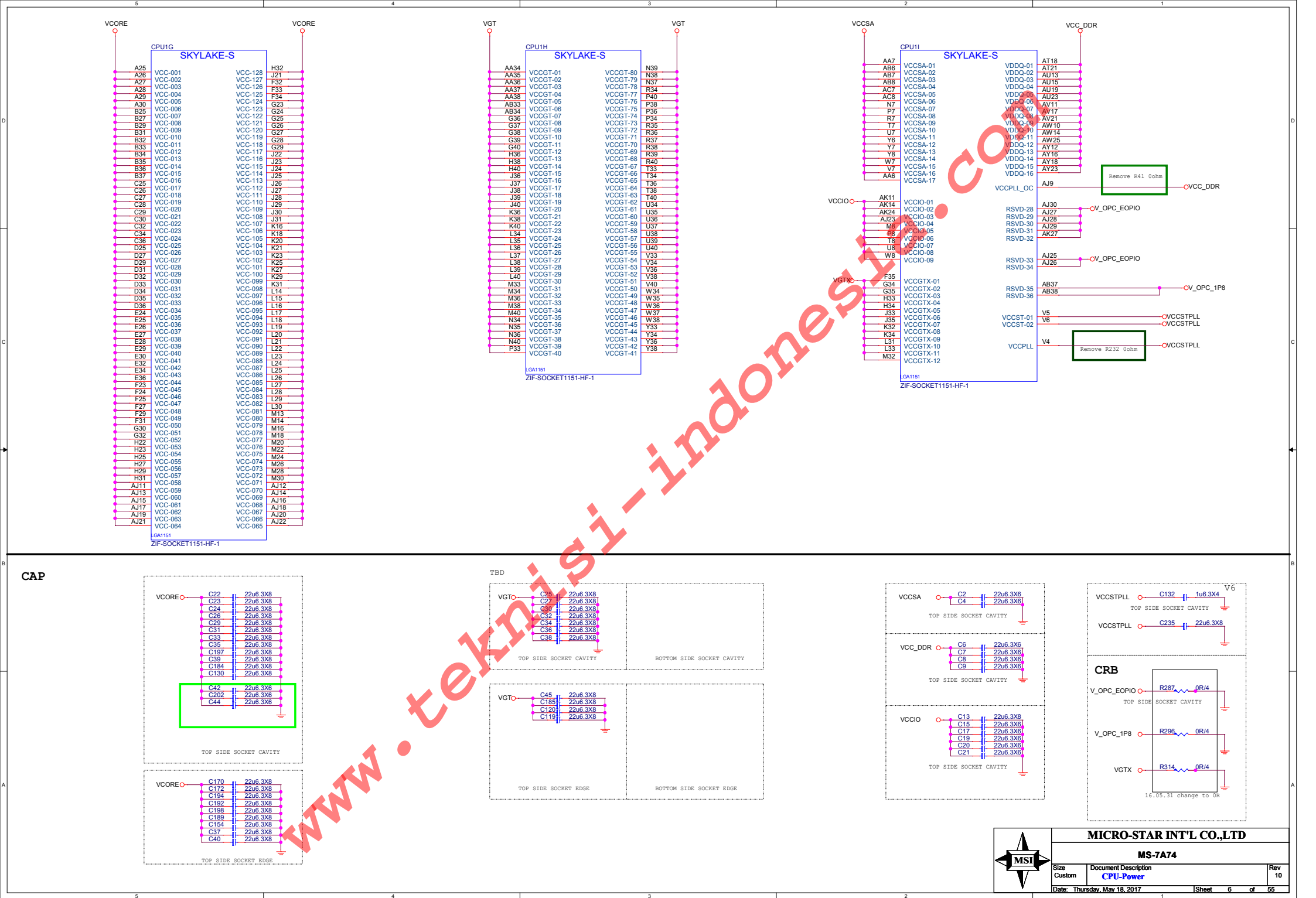


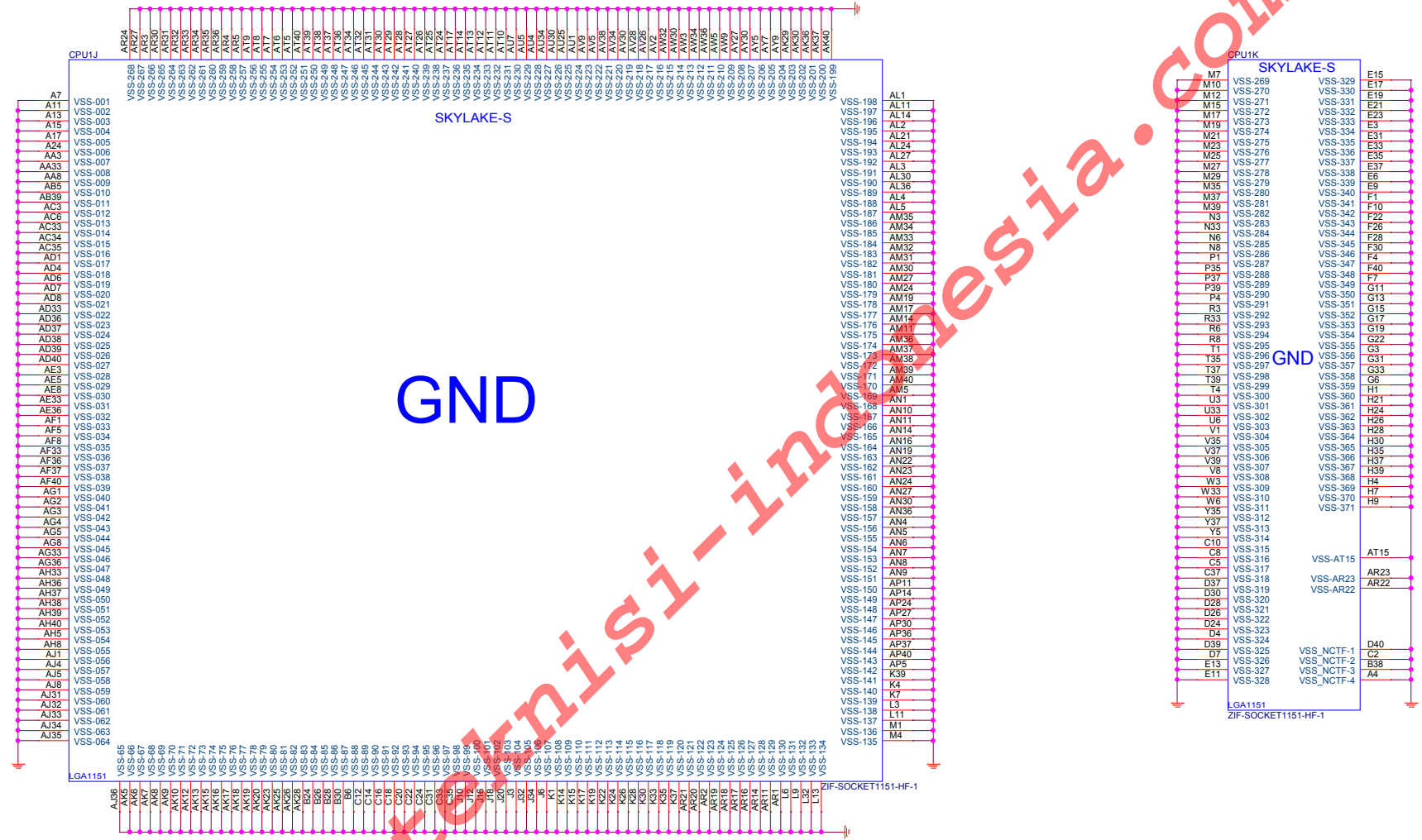


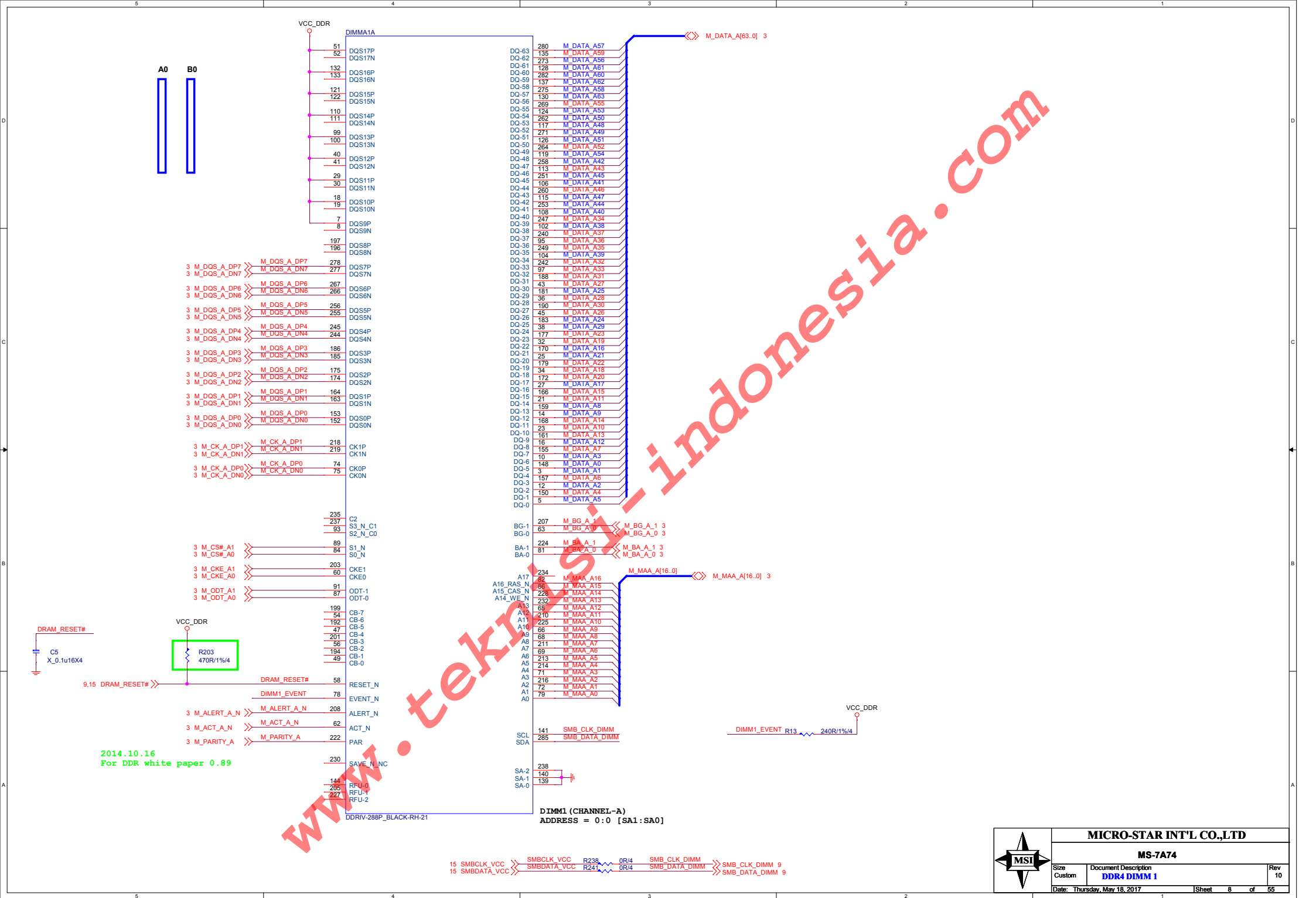


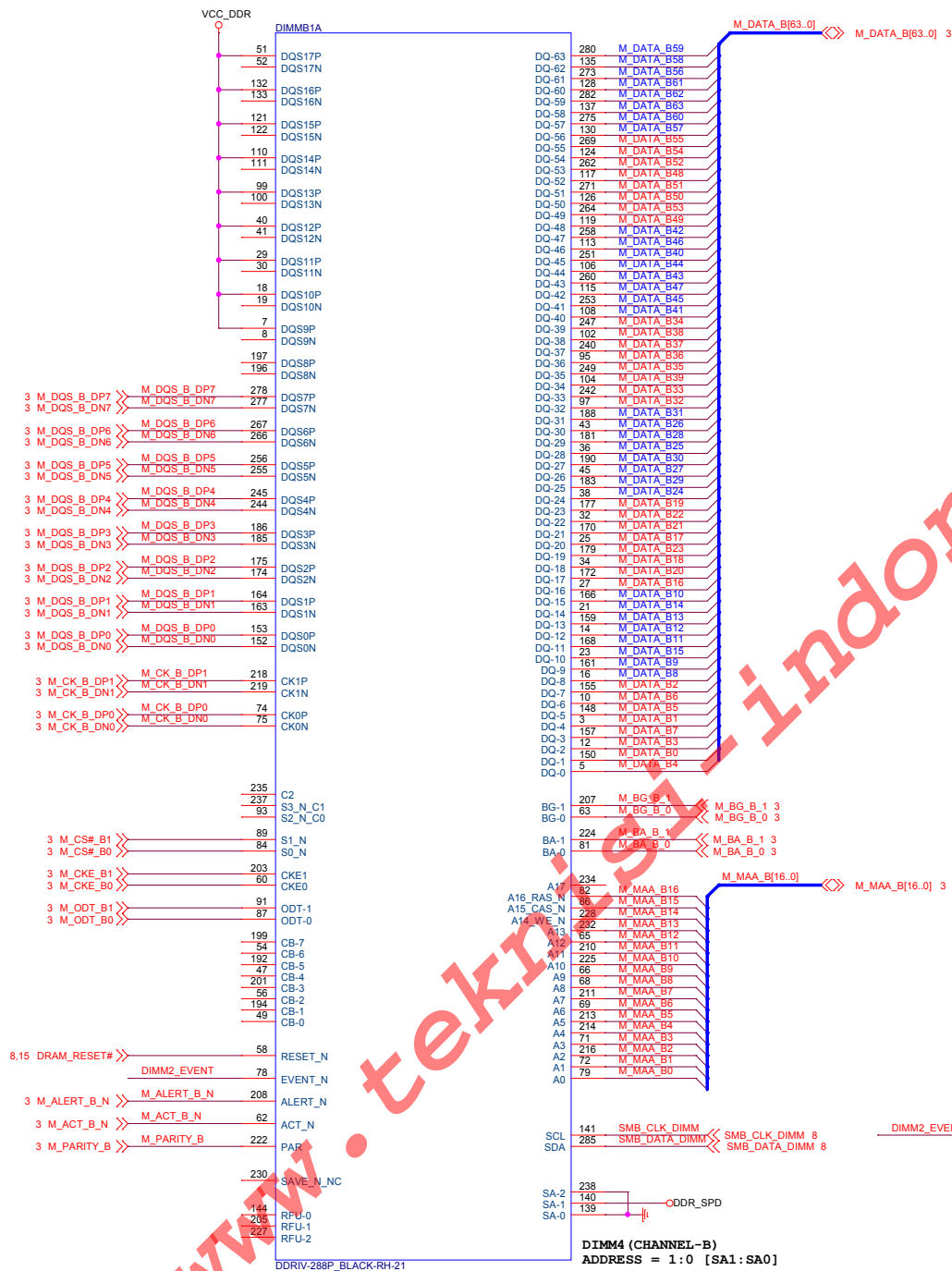
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			MS-7A74	
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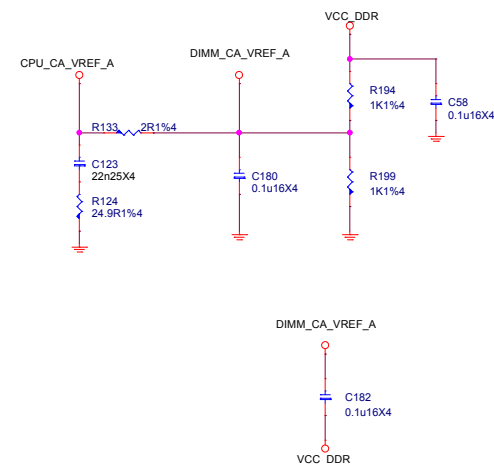
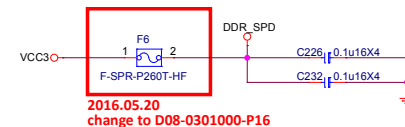
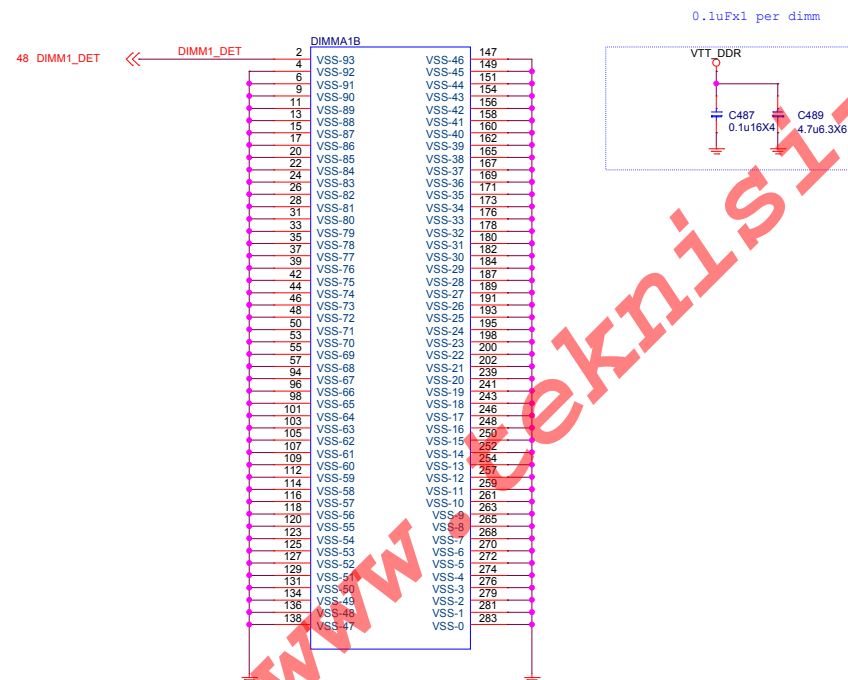
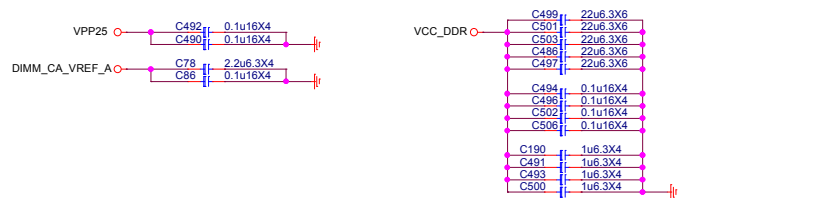
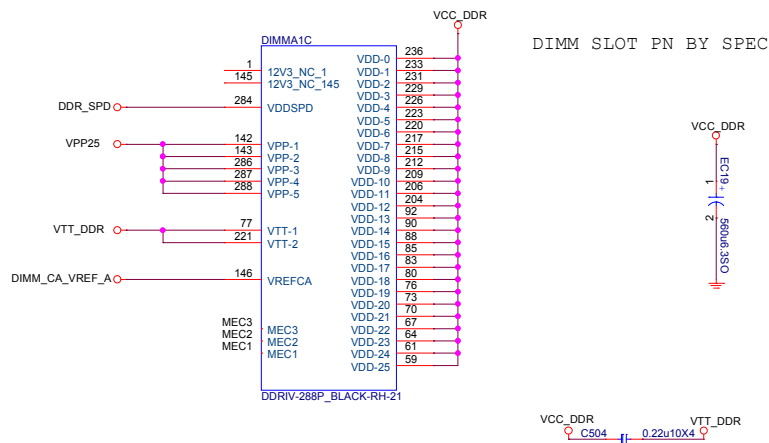


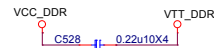
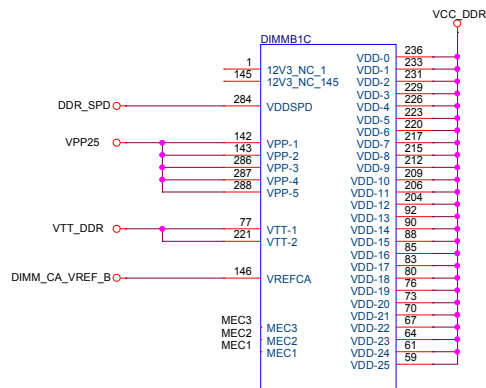


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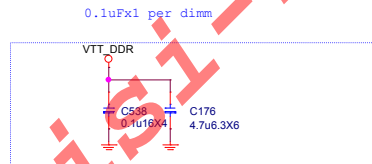
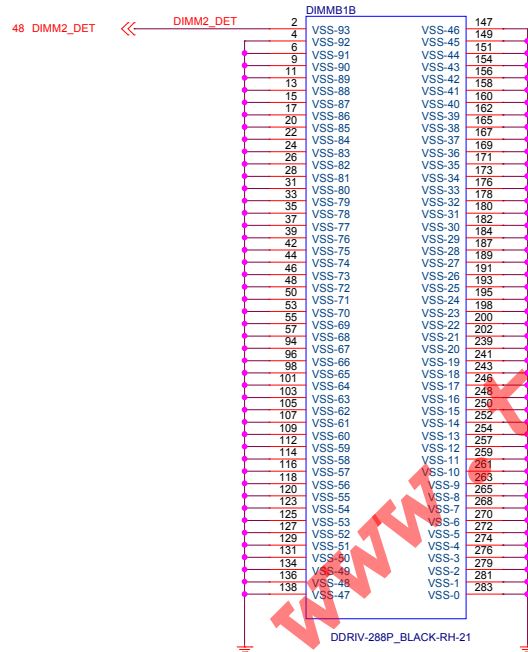
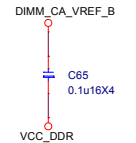
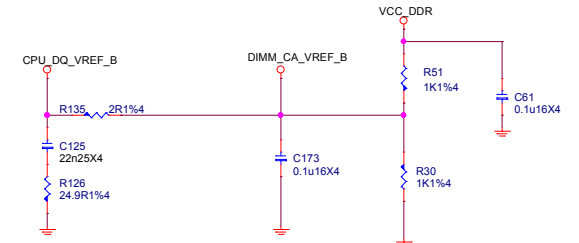
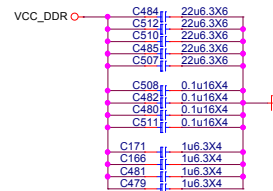
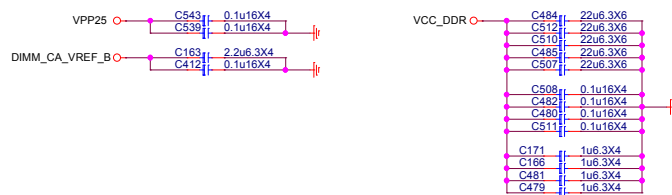
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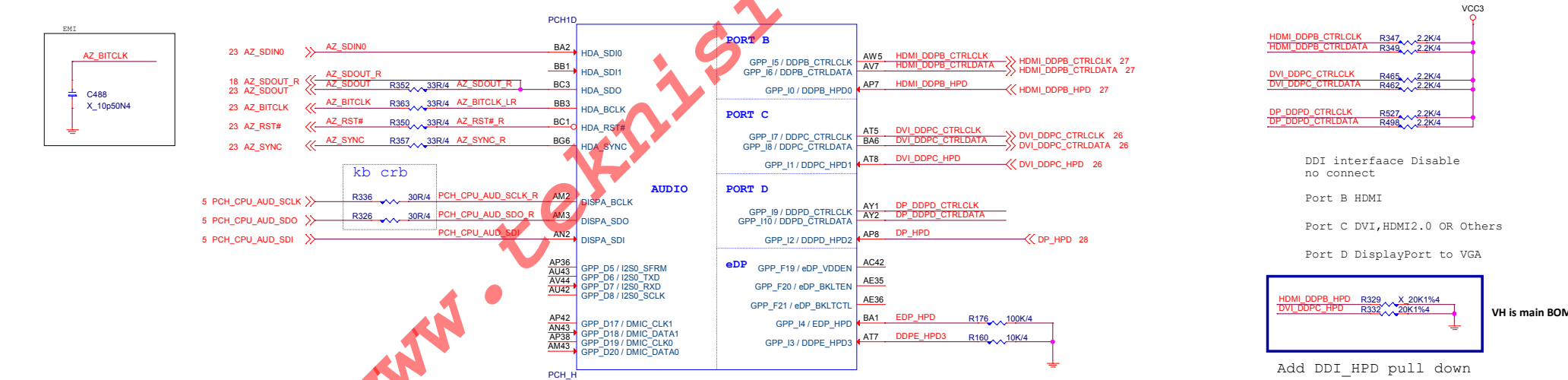
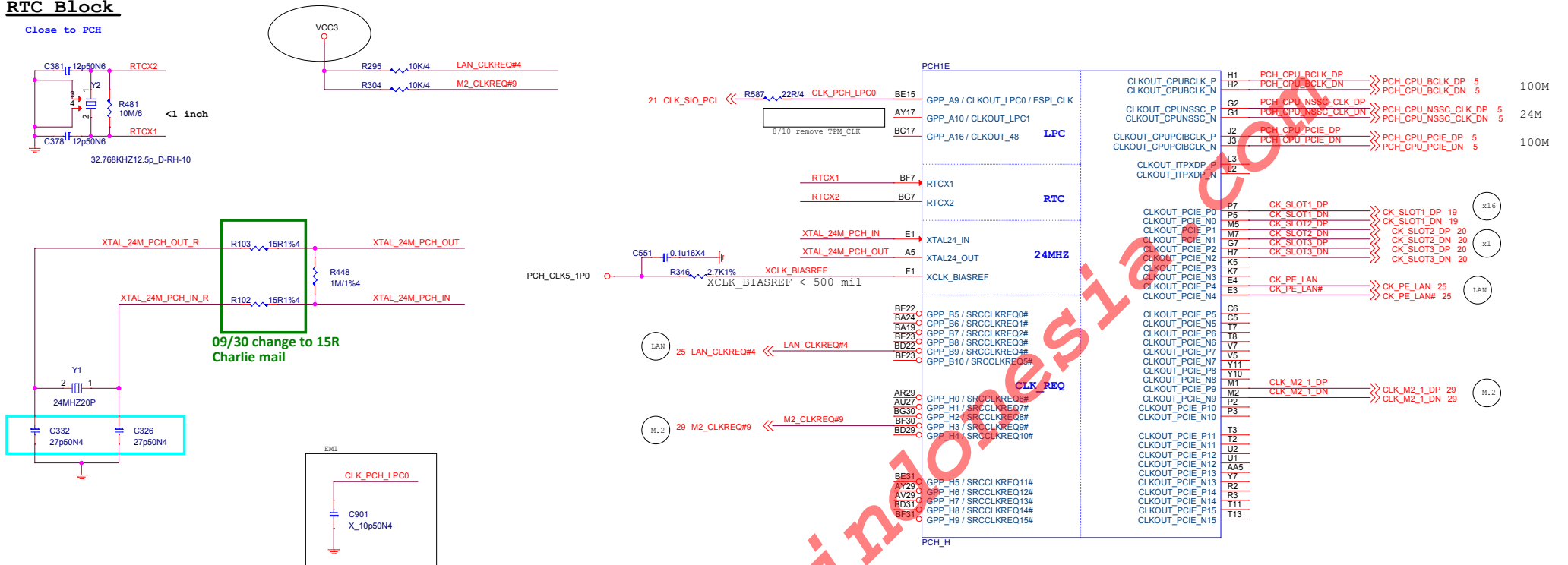


Place close to DIMM2

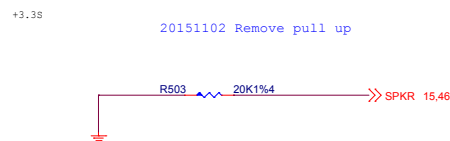


RTC Block

Close to PCH

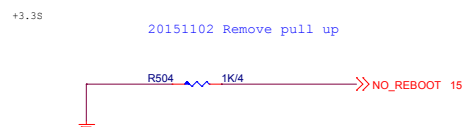


TOP Swap



Internal pull-down 20K is disabled after PLTRST#

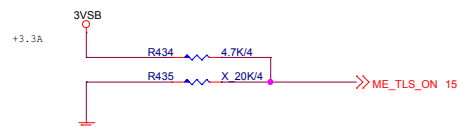
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down 20K is disabled after PLTRST#

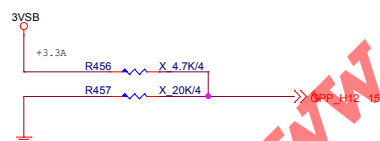
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down 20K is disabled after RSMRST

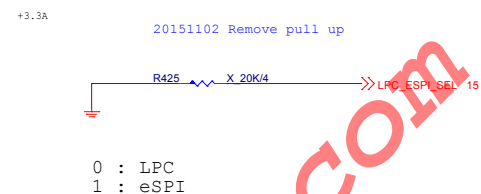
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down 20K is disabled after RSMRST

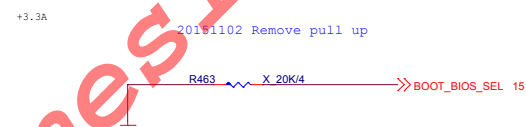
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down 20K is disabled after RSMRST

Boot BIOS

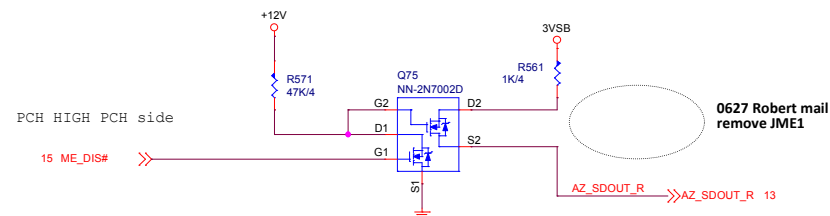


0 : SPI
1 : LPC

Internal pull-down 20K is disabled after PLTRST

HDA_SDO

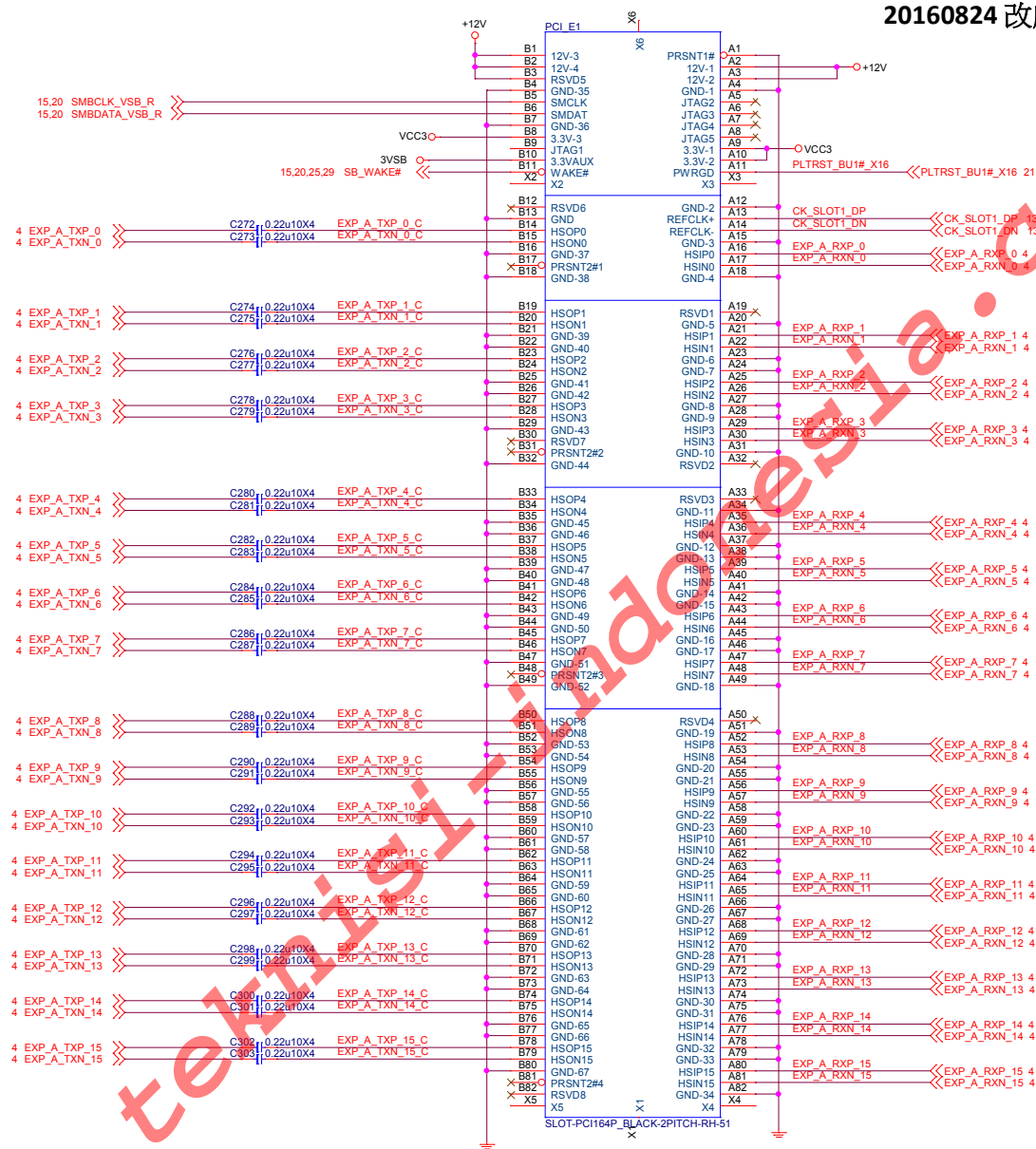
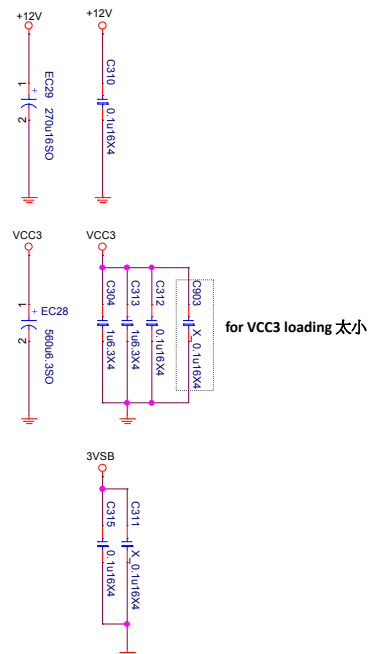
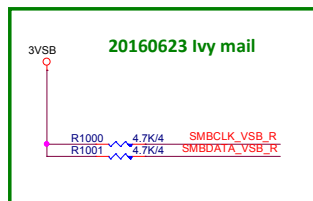
ME flash by GPIO



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Custom	PCH-Strap	10
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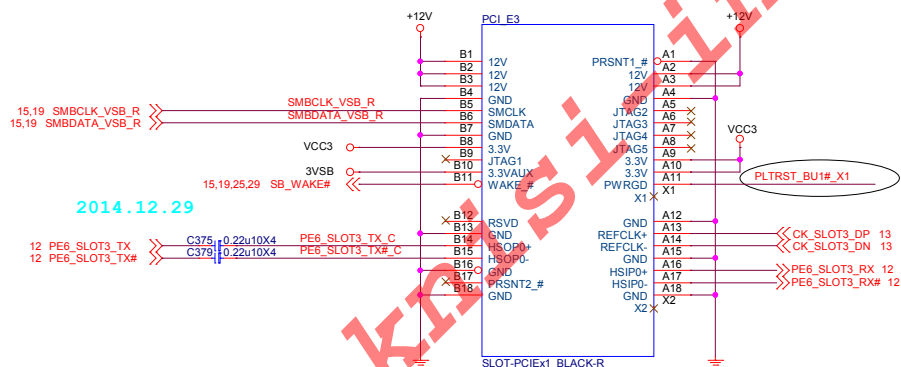
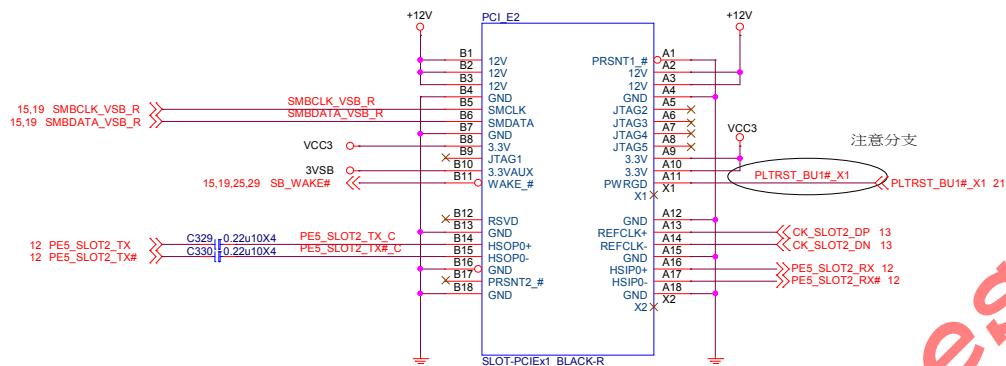


MICRO-STAR INT'L CO.,LTD

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Size	Document Description
Custom	PCIE SLOT-CPU(X16)

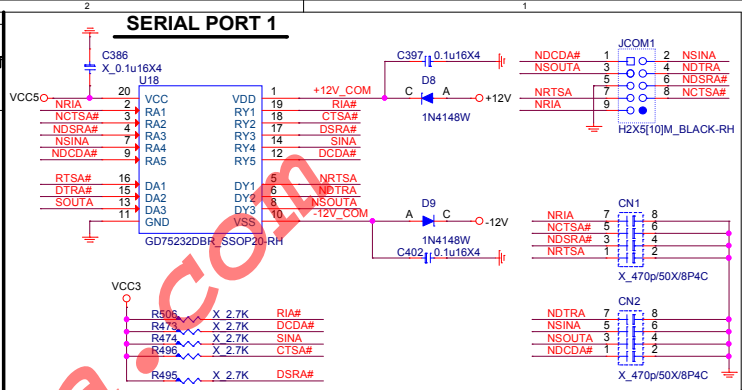
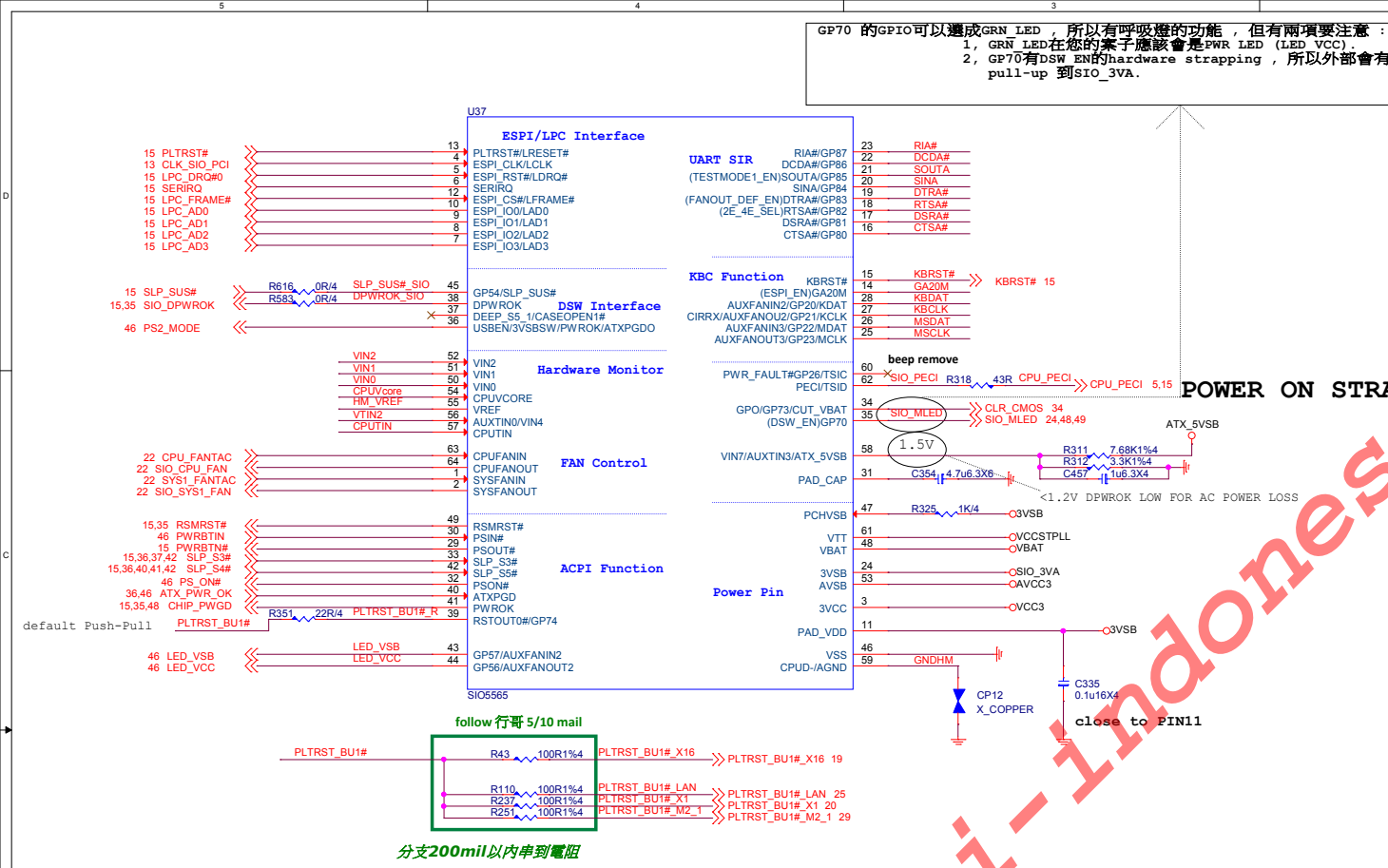
Rev	10
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Custom	PCIE SLOT-PCH(X1)	10
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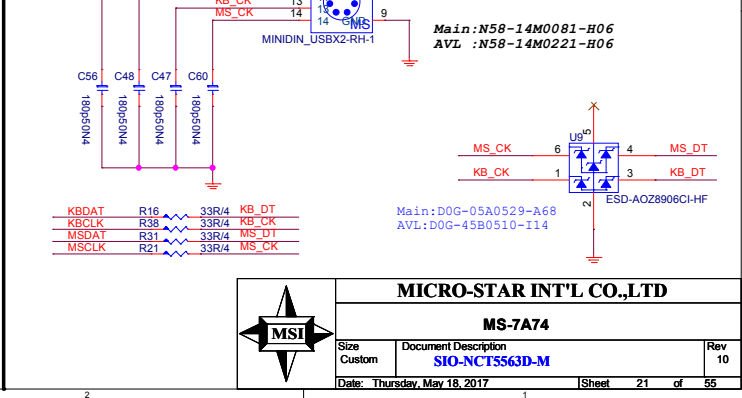
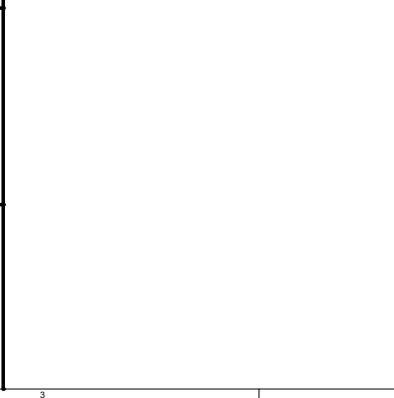
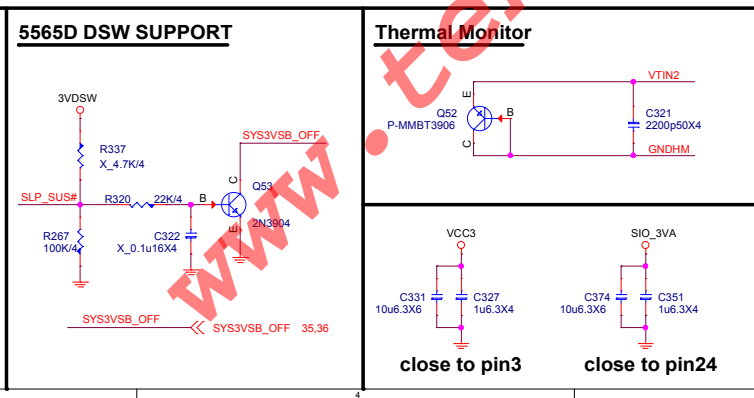
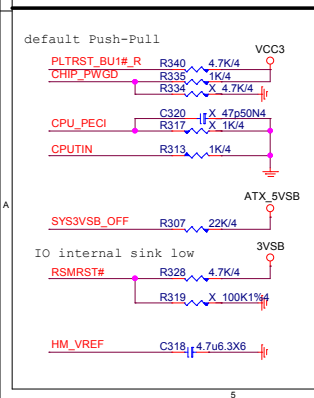
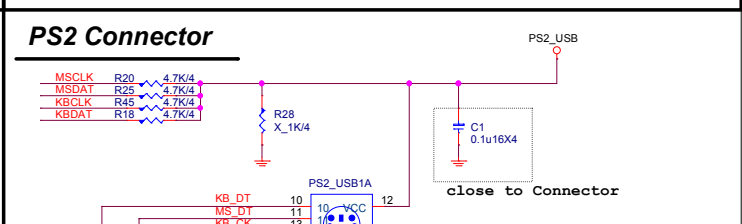
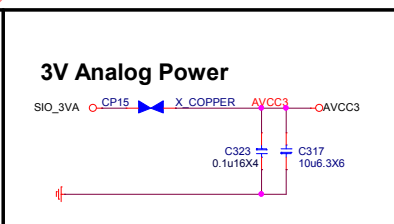
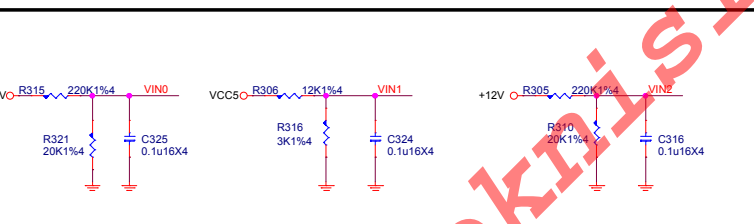
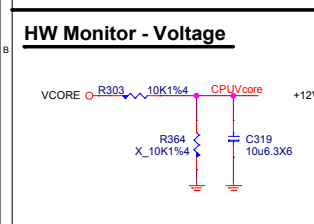
POWER ON STRAPPING PIN FOR NCT5565D

PIN	5563D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	CPU FANOUT default RPM 50%	CPU FANOUT default RPM 100%
21	TESTMODE1_EN	SOUTA	DISABLE TESTMODE	ENABLE TESTMODE
14	ESPI_EN	GA20M	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	DISABLE	ENABLE DSW_EN

close to Connector

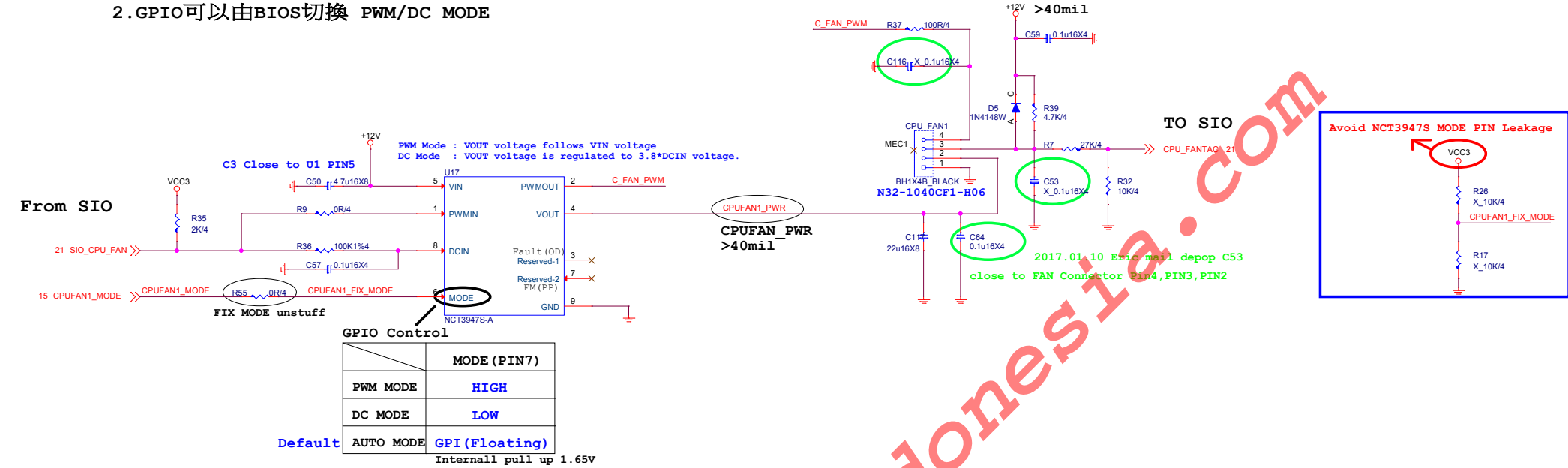
Main: N58-14M0081-B06

AVL: N58-14M0221-B06



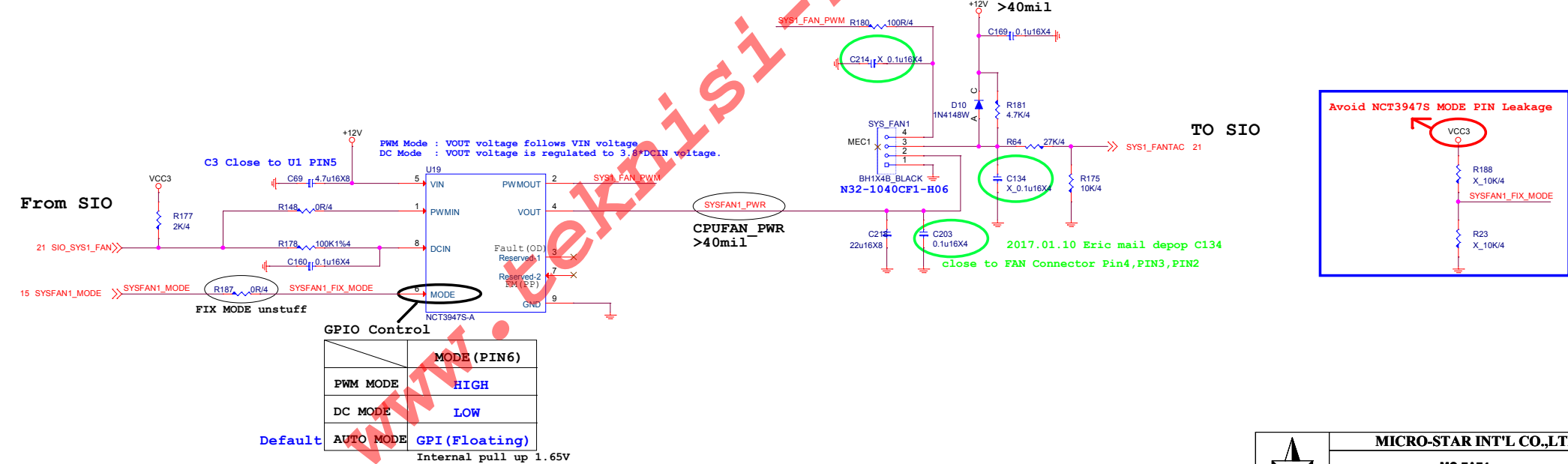
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE

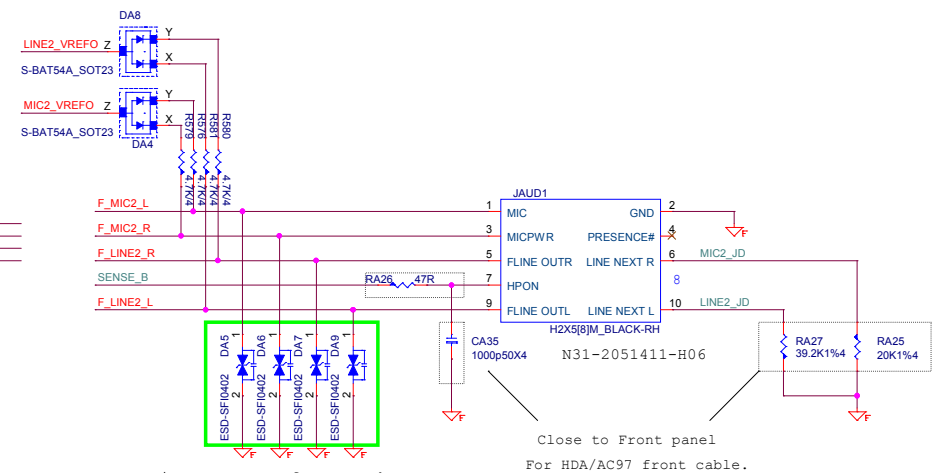
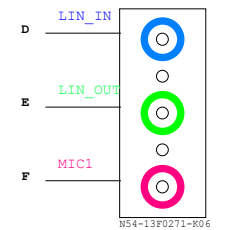
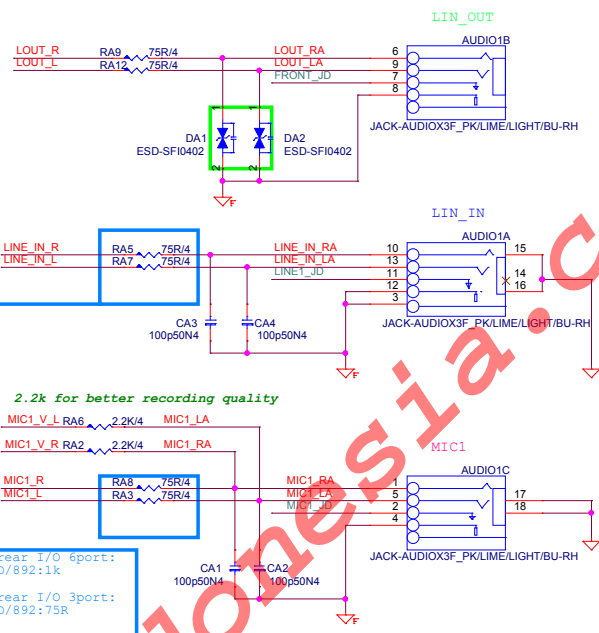
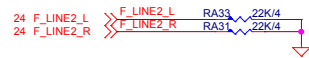
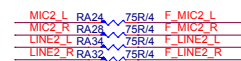
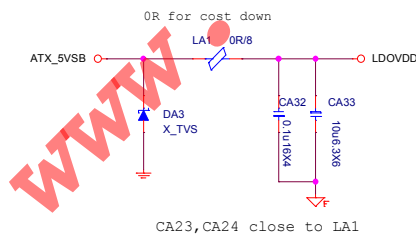
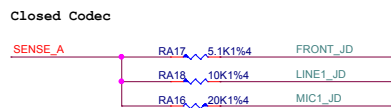
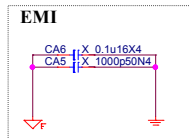


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



Closed code 2015/6/22



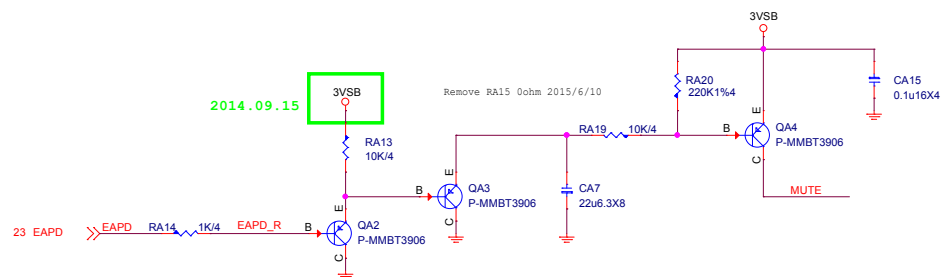
D0G-2950500-SI0
D0G-3010510-I05
Close to Jack



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Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

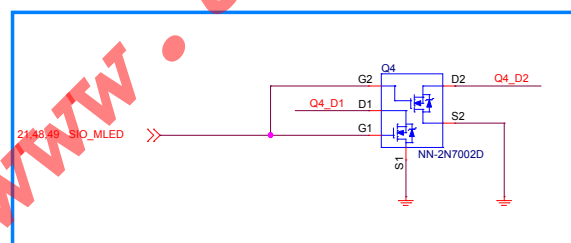
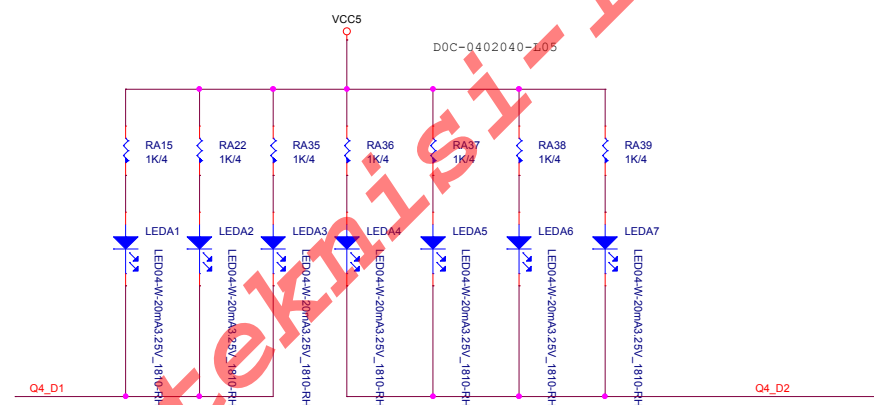


Digital

Analog



Audio LED



2016.01.12:Modify Q4 to Dual 7002 & Remove OR

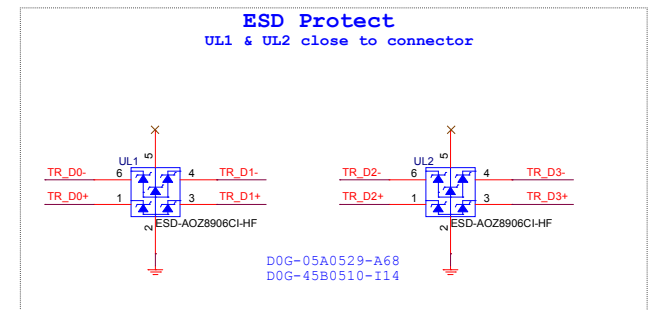
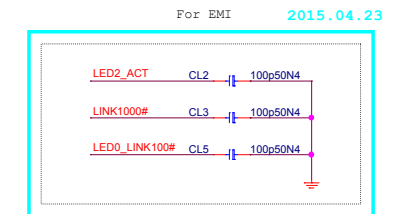
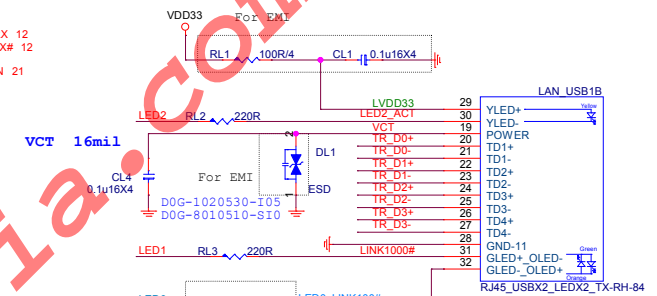
RTL8111G/RTL8111H Giga LAN

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

2016.08.26 崑山反應

LAN_CLKREQ#4_R R1014 0R/4 LAN_CLKREQ#4 13

LAN Connector



8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDFS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDFS	5.50	18.15

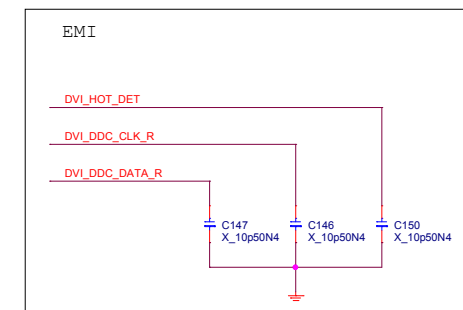
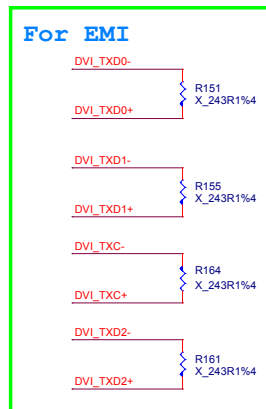
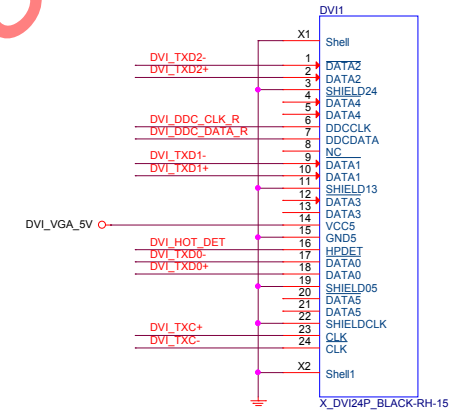


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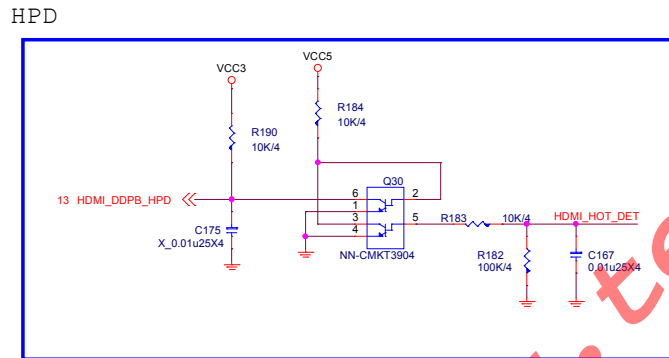
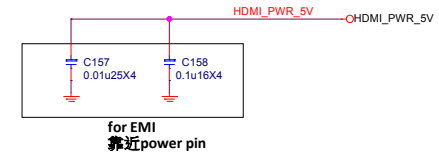
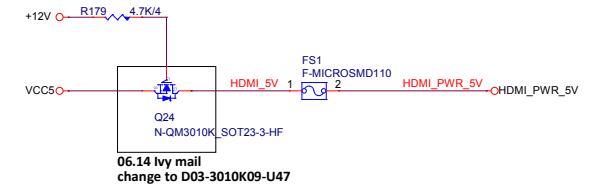
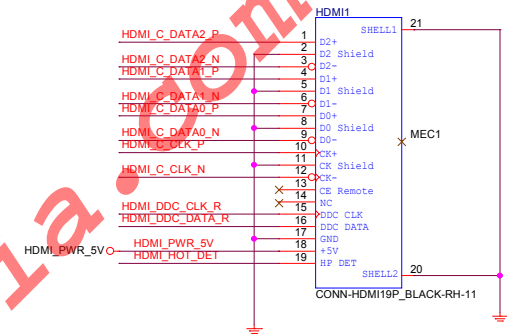
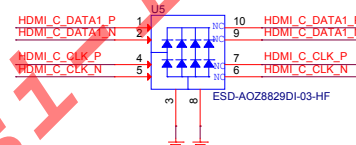
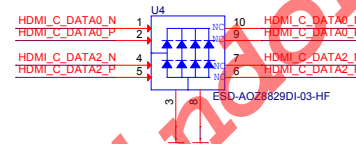
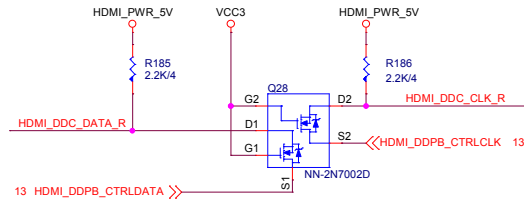
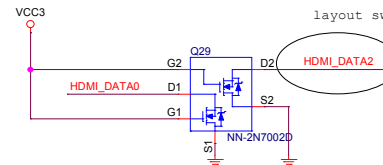
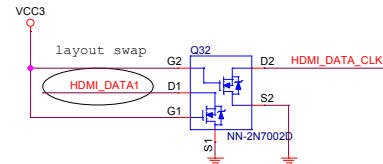
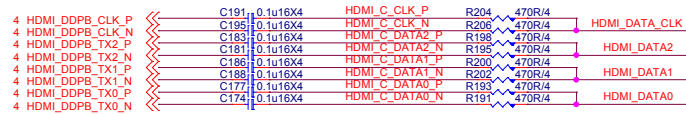
MS-7A74

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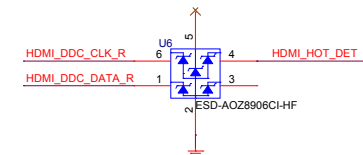
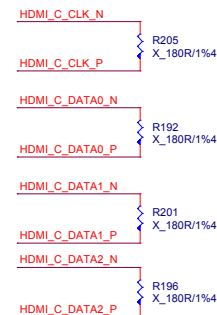
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



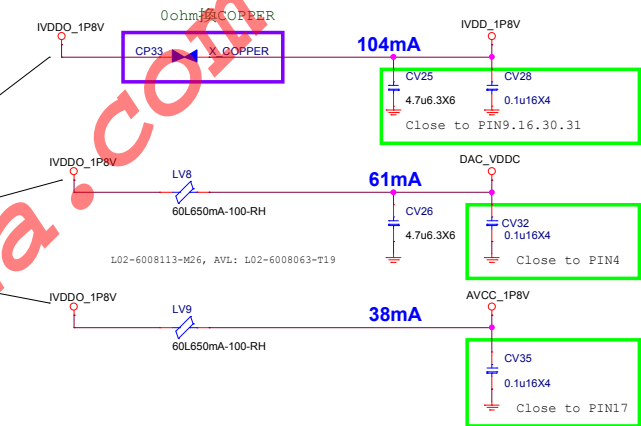
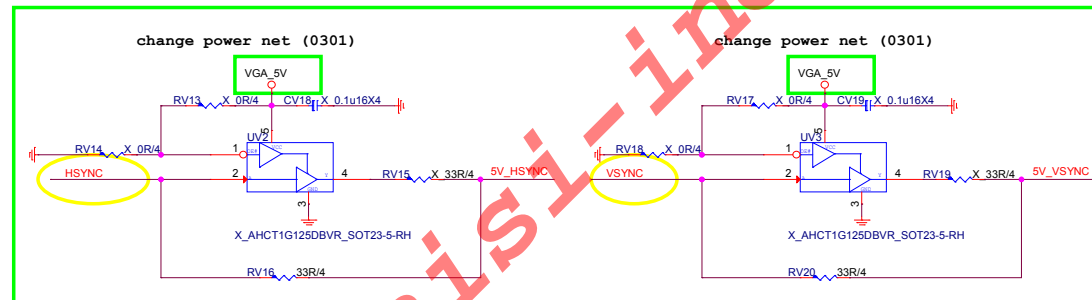
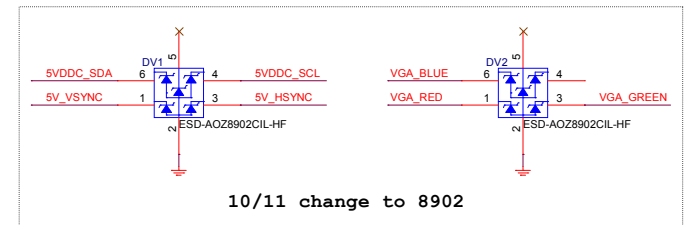
For EMI



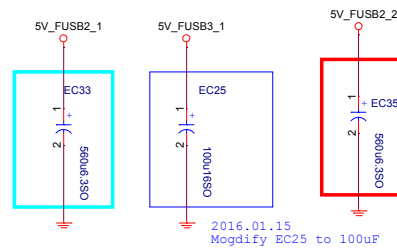
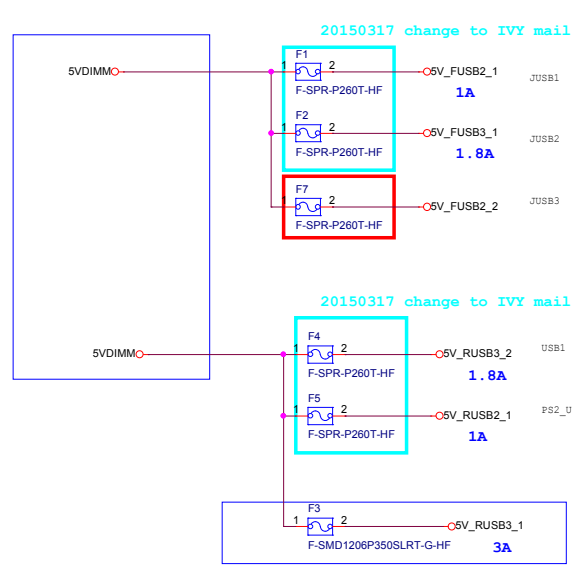
If connect to eDP port, must confirm whether it support hot plug detection HPD and re-auxtraining



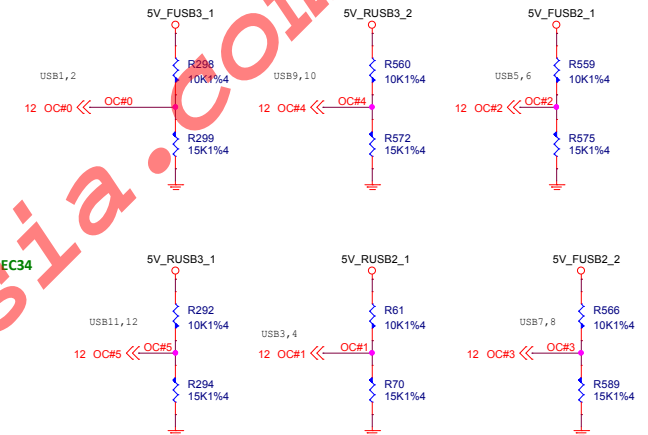
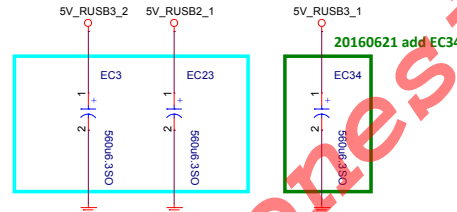
System Status	GPIO	IT6516b's HPD
Legacy Mode (VBIOS) /DOS Mode	HIGH	Force HIGH
Windows /UEFI Mode (GOP)	LOW	Depend on VGA device's plug/unplug

[illegible]

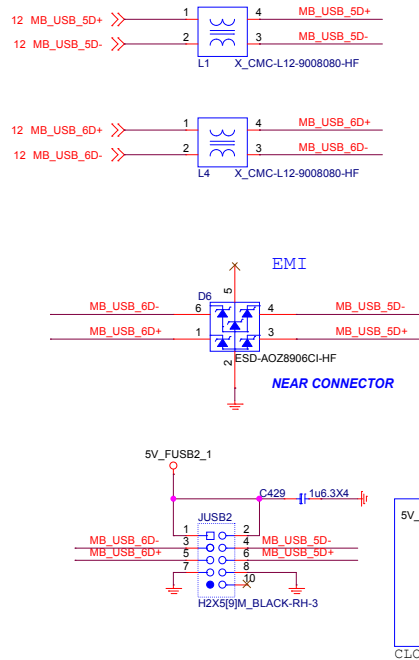
20151105 Modify to 5VDIMM



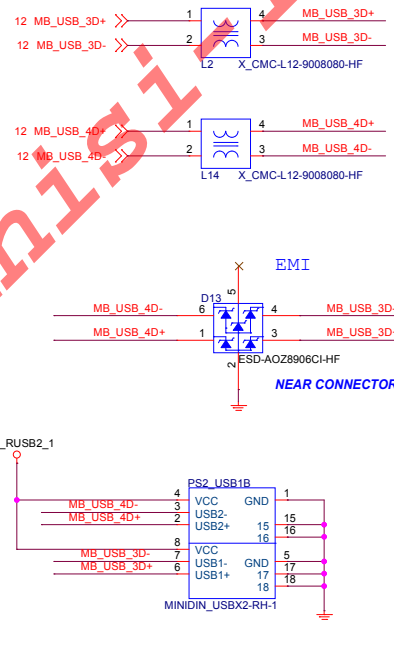
20150924 change USB CAP



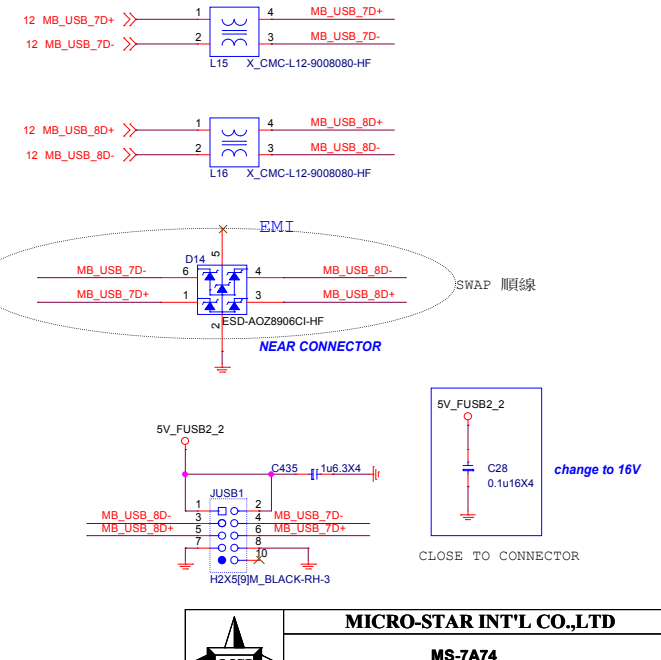
FRONT JUSB2 PORT 5,6



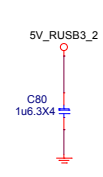
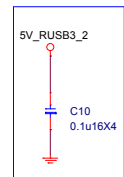
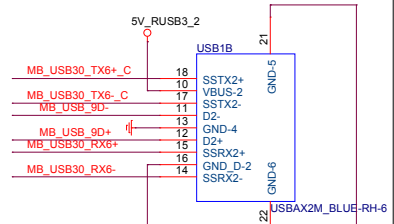
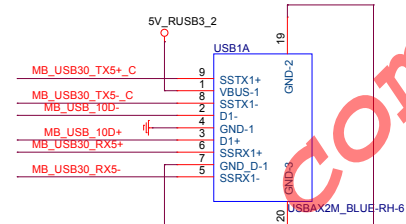
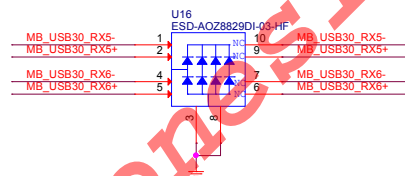
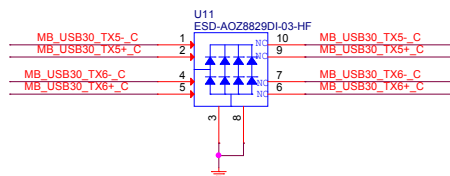
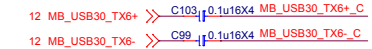
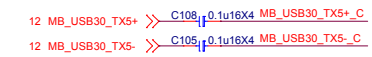
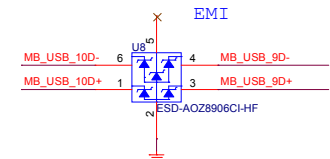
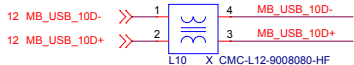
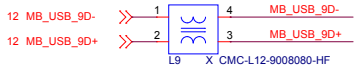
PS2_USB1 PORT 3,4



FRONT JUSB1 PORT 7,8

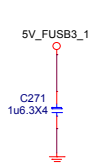
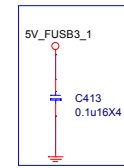
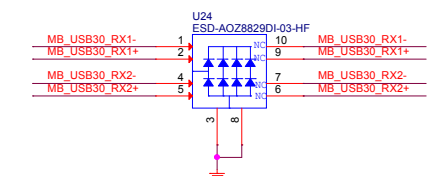
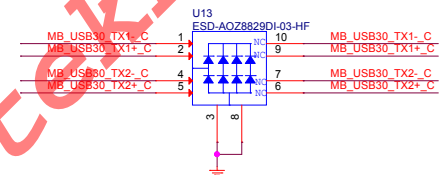
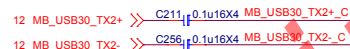
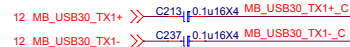


Rear USB1 port 9,10



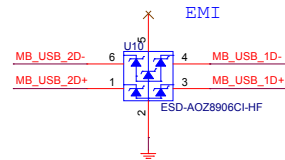
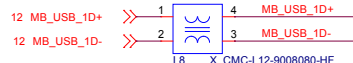
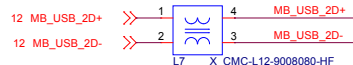
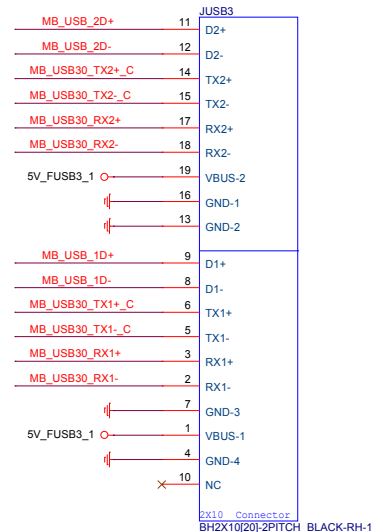
CLOSE TO CONNECTOR

Front JUSB3 port 1,2



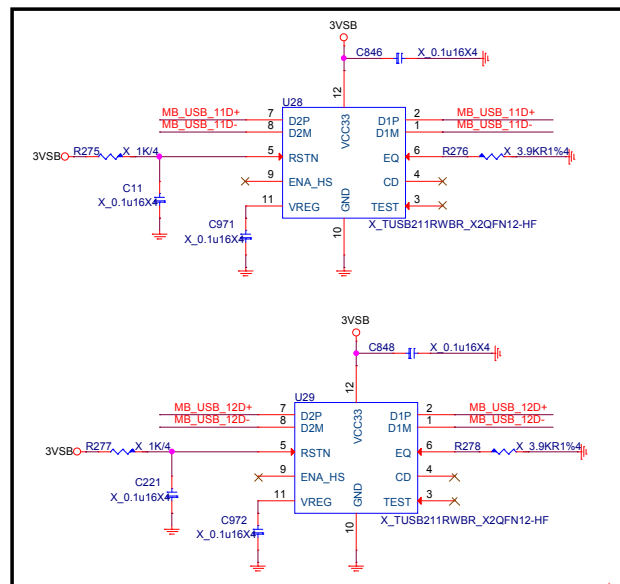
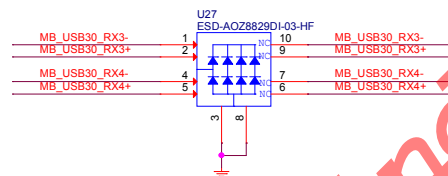
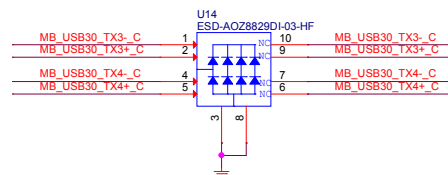
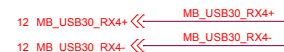
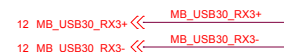
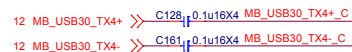
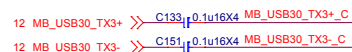
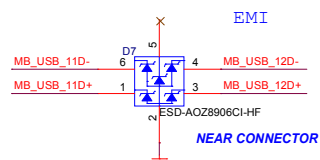
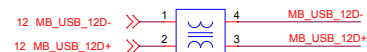
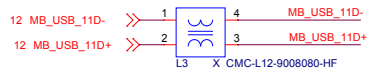
CLOSE TO CONNECTOR

10/06 change to N32-2101091-H06

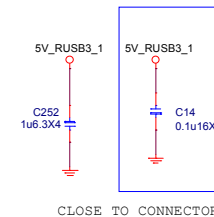
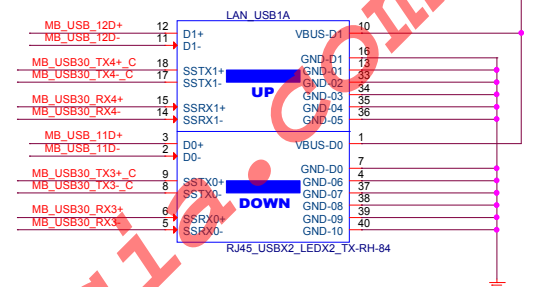


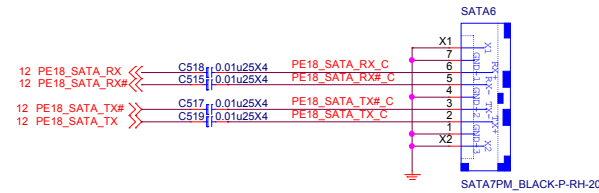
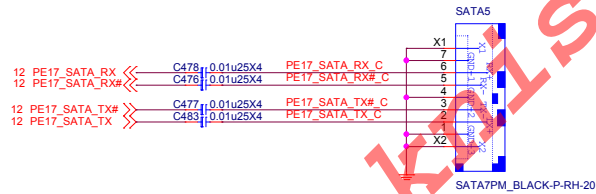
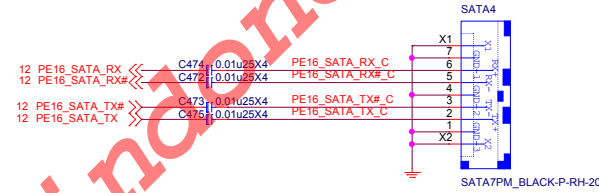
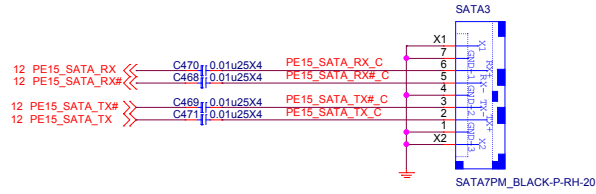
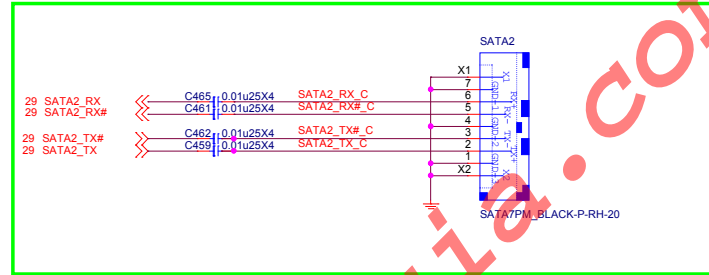
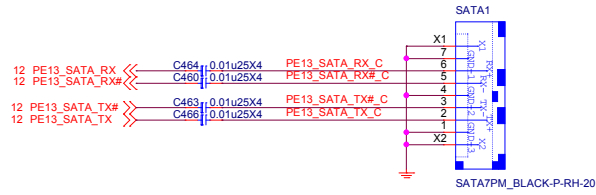
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LAN_USB port 11,12



2016.05.30 PM add VR function
2016.09.23 remove VR



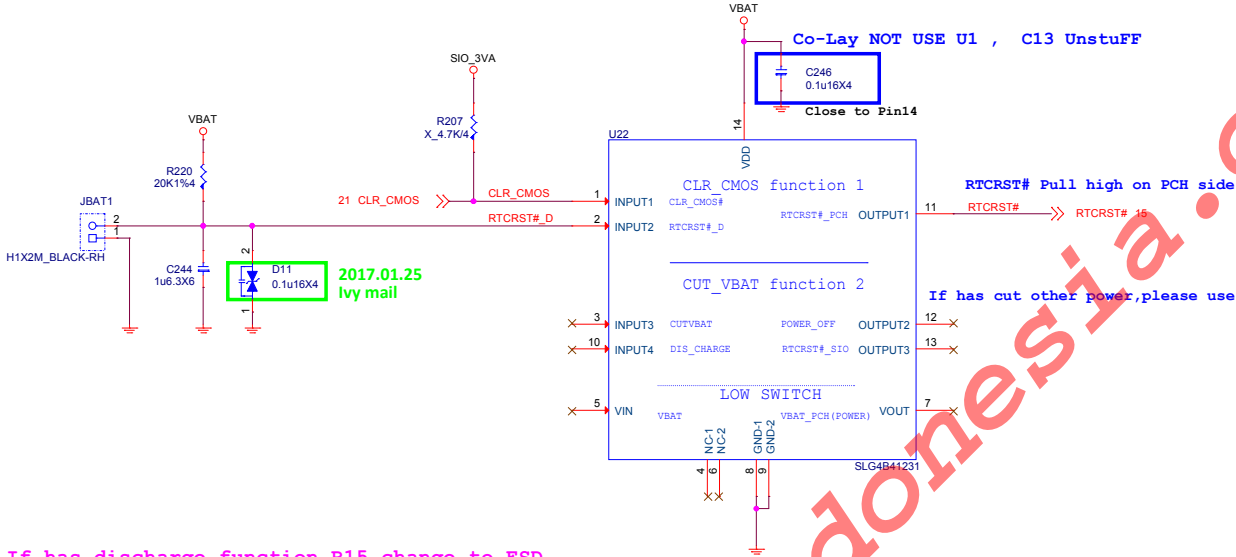
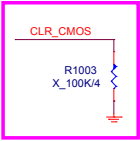


CLR_CMOS



If STUFF R20 Please Check RTCRST# Double Pull High

20160629

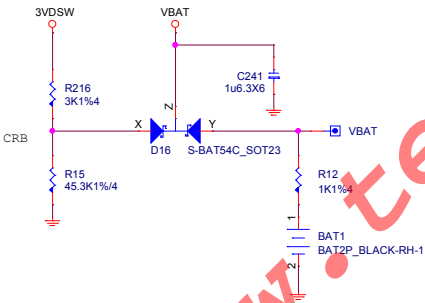


If has discharge function R15 change to ESD.
ESD"D0G-2950500-SI0"

Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

VBAT

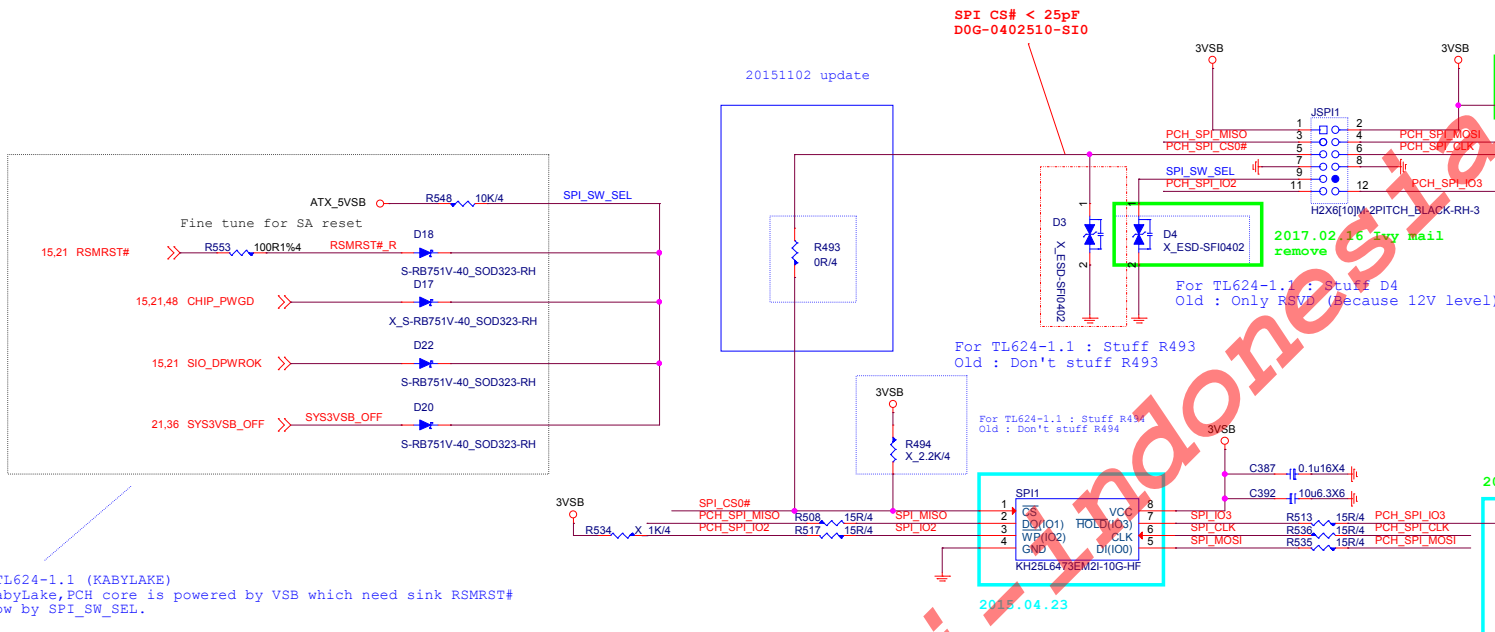


Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

Co-Lay NOT USE U1 , R20 STUFF

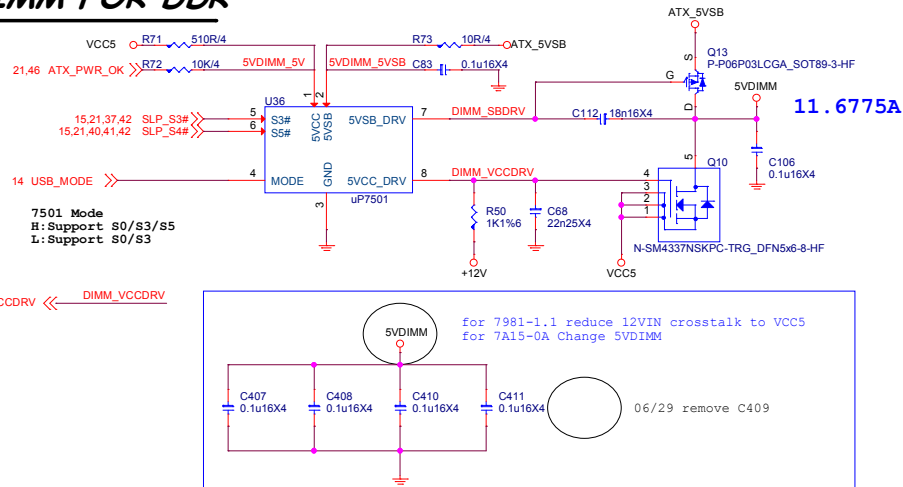
15 PCH_SPI_MOSI << PCH_SPI_MOSI
15 PCH_SPI_MISO << PCH_SPI_MISO
15 PCH_SPI_CLK << PCH_SPI_CLK
15 PCH_SPI_CS0# << PCH_SPI_CS0#
15 PCH_SPI_I02 << PCH_SPI_I02
15 PCH_SPI_I03 << PCH_SPI_I03



- * if you not support Standby power in S5 Status, component Q14.G Pull-high to +12V & Q14 MOS select 2N7002
 - * if you support Standby power in S5 Status (Ex: ECH is B75 Chipset), component Q14.G Pull-high to ATX_5VSB, Q14 must select "Vth" under 1V (Component Suggestion as below)
- D03-0341409-A68 / D03-0230019-A30

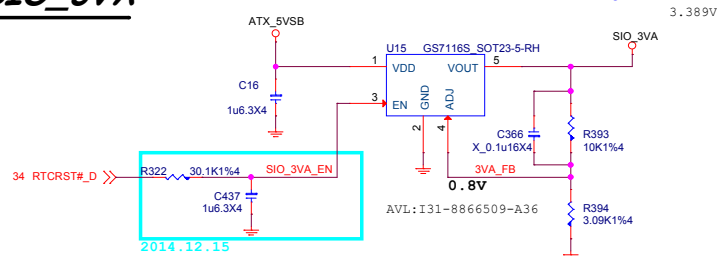
5VDIMM FOR DDR

(3A for DDR, 6.6A for USB)



SIO_3VA

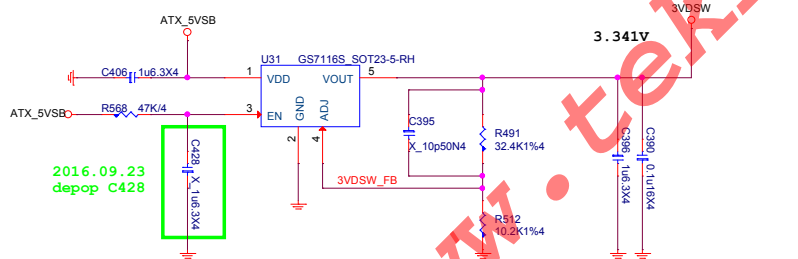
20mA



3VDSW

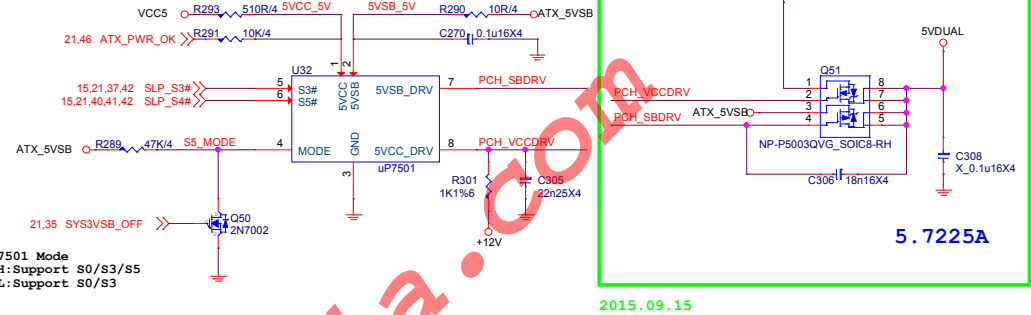
20151110 Modify to GS7116

204mA



5VDUAL

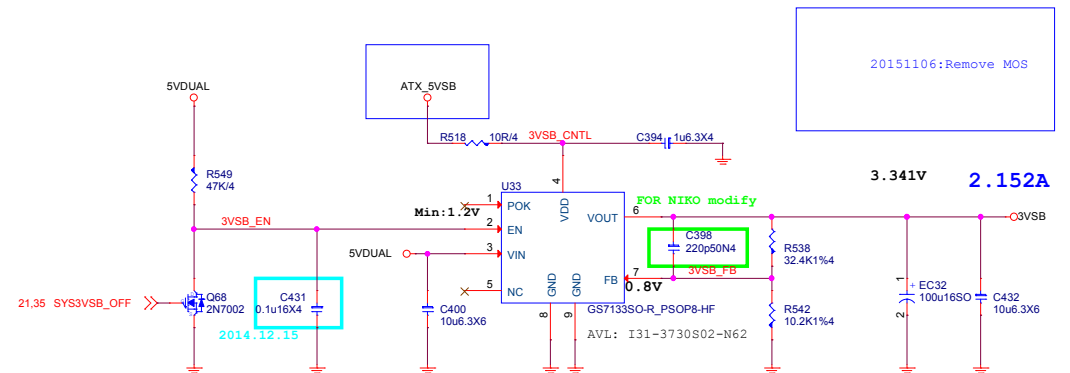
5VDUAL is power source of 1P0SB, 1.8PSB & 3VSB



For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 PCH VCCDRV work when the VCC5 ready
(When VCC5 up to 4.72V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

20151106 :Remove 3VSB Patch Circuit

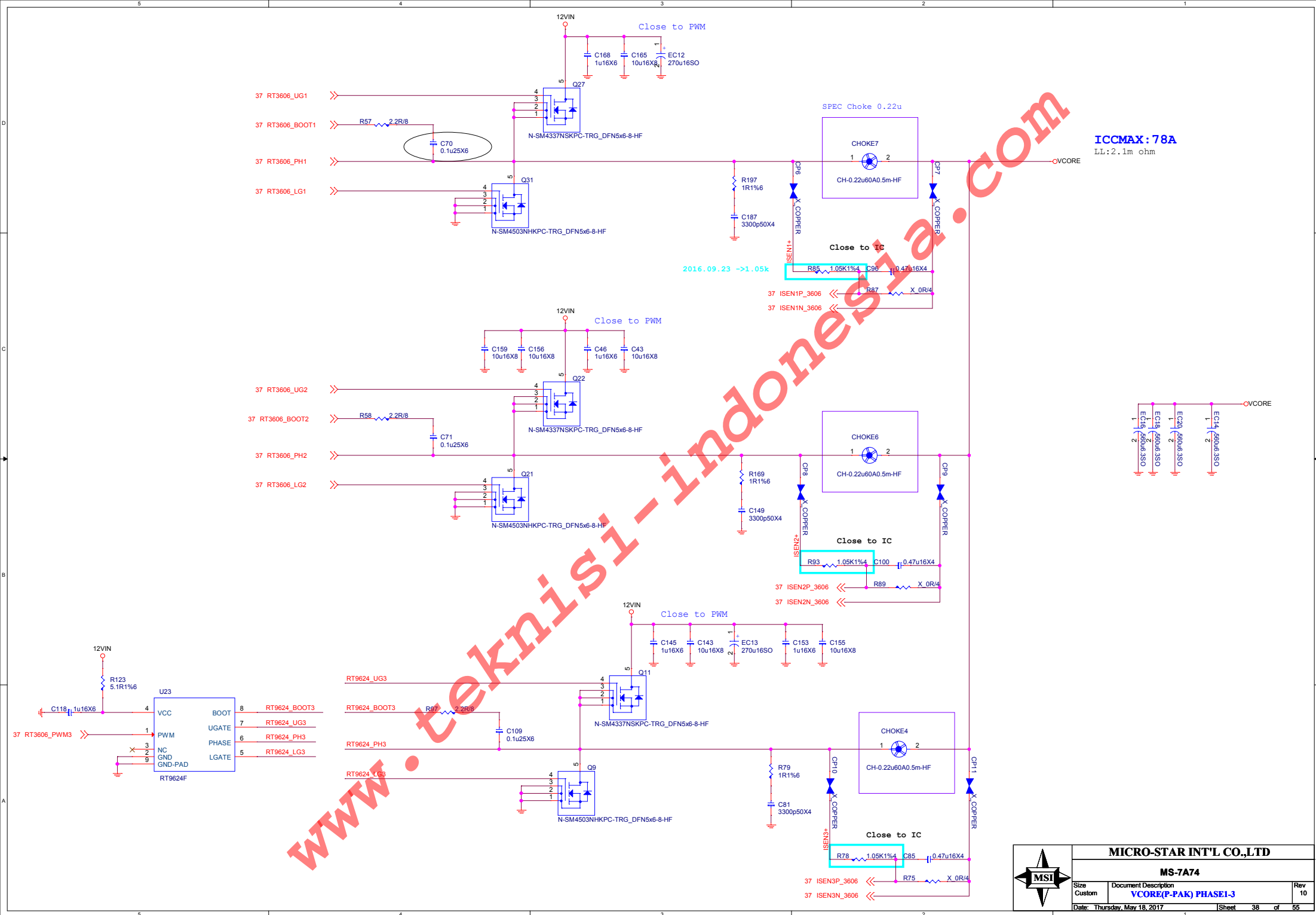
3VSB cost down

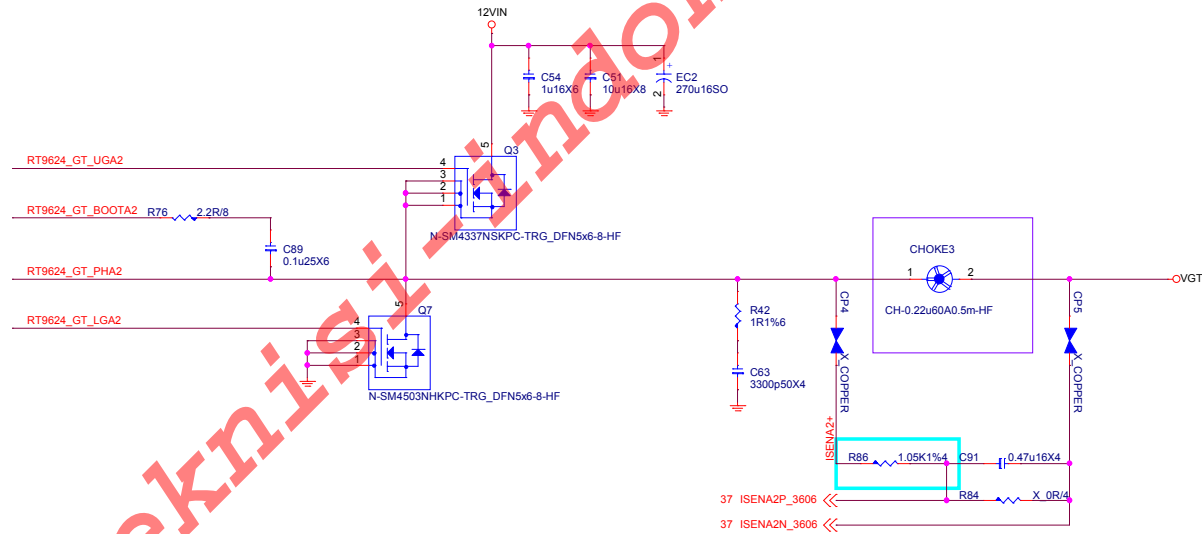
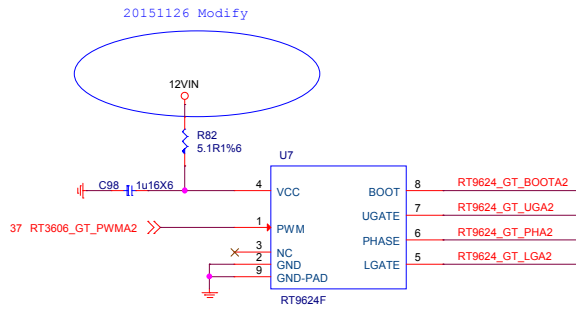
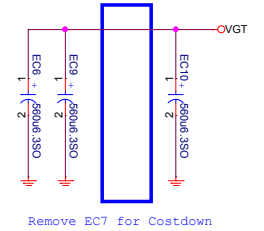
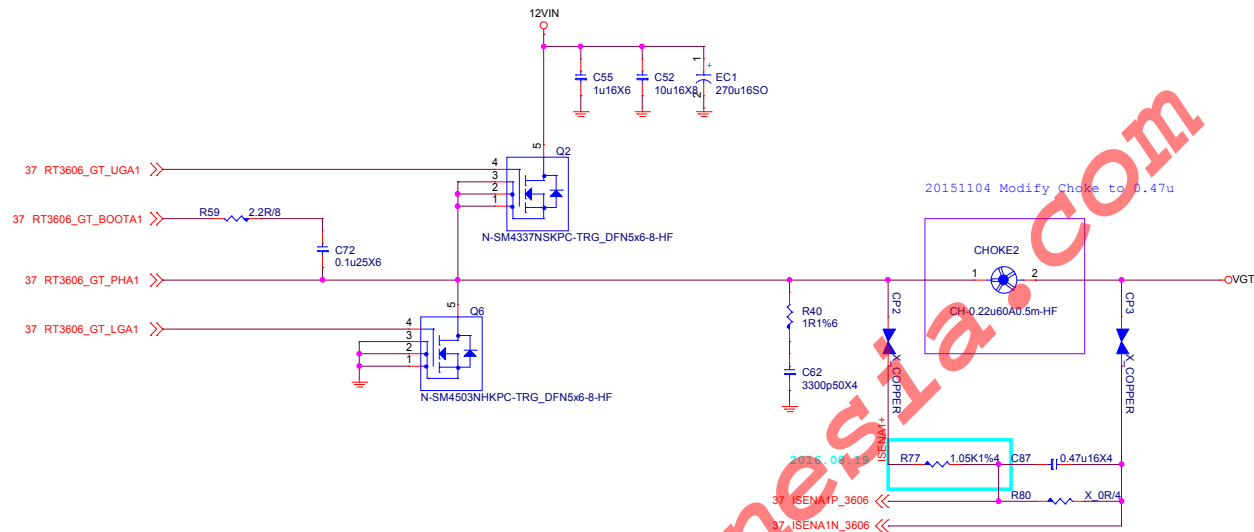
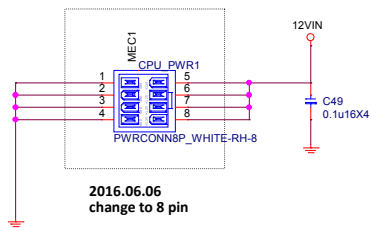


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DDR4_1.2V 2.8A+ 4.75A+0.375A=7.925

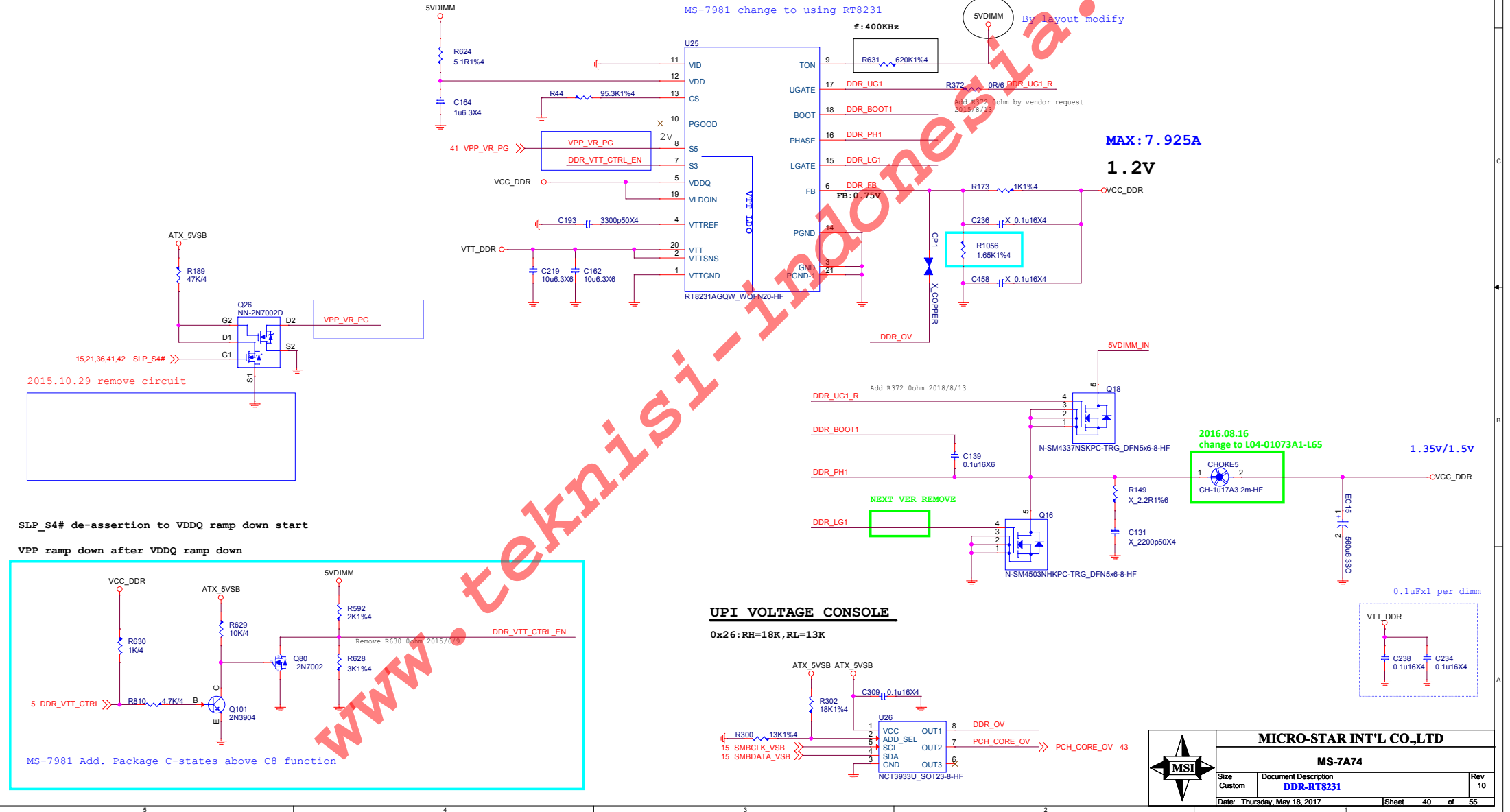
2.8A FOR CPU
4.8A FOR 2DIMM DDR3
0.375A FOR VTT_DDR

OCP = 7.925A * 1.5 = 11.8875A
Current limit = 95.3K(R1054) * 5uA / 10 / 4mohm = 11.91A

2015.04.23 change to RT8231

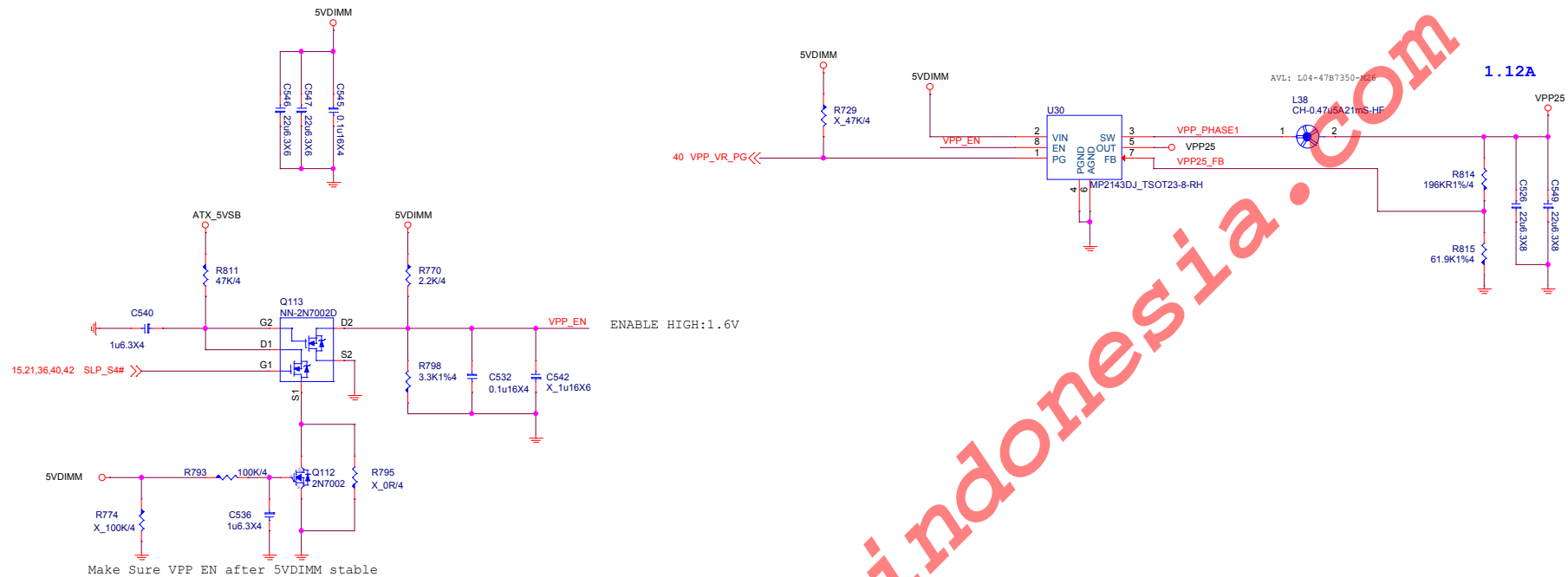
VID	Reference Voltage (V)
H	0.675
L	0.75

$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$
 $= 7.925 * 0.42$
 $= 3.384A$



2DIMM :1.12A FOR DDR VPP2.5V

VPP25 Power
2.5V; 1.12A

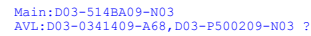


MICRO-STAR INT'L CO.,LTD

MS-7A74

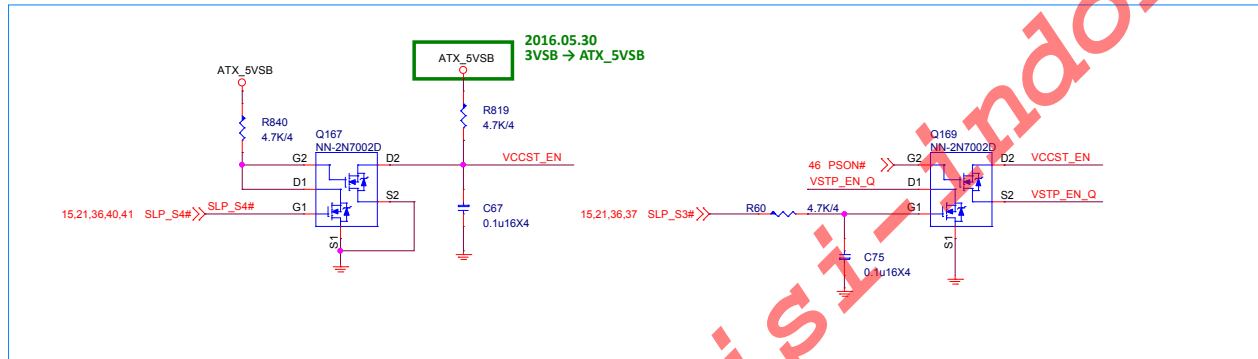
Size Custom	Document Description DDR-MP2143-VPP25	Rev 10
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For Cost down VCCST&VCCPLL merge



VCCIO ramped and stable before
beginning of VCCOPC/VCCEPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD



PCH 1VSB

1.0V; 8.572A+5.5A+0.21A=14.282

OCP =21.423A

Rocset = 1.5 * I_{max} * R_{dson(1ow)} / I_{ocset}
 = 1.5 * 14.282 * 3.6mohm / 10uA
 =7.71K

Rocs: 7.68K, OCP:

D03-4C05N03-005 : 15.36A

D03-632BA0C-N03 : 16.69A

when use UBIQ MOS Rocs:7.68K OPC:21.33A

R_{dson(1ow)} 4.5V

D03-4C05N03-005 : 5 mohm

D03-632BA0C-N03 : 4.6 mohm

D03-3116M00-U47 : 3.6mohm

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

MAX: 14.282A

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.8335uH (K = 30\%)$$

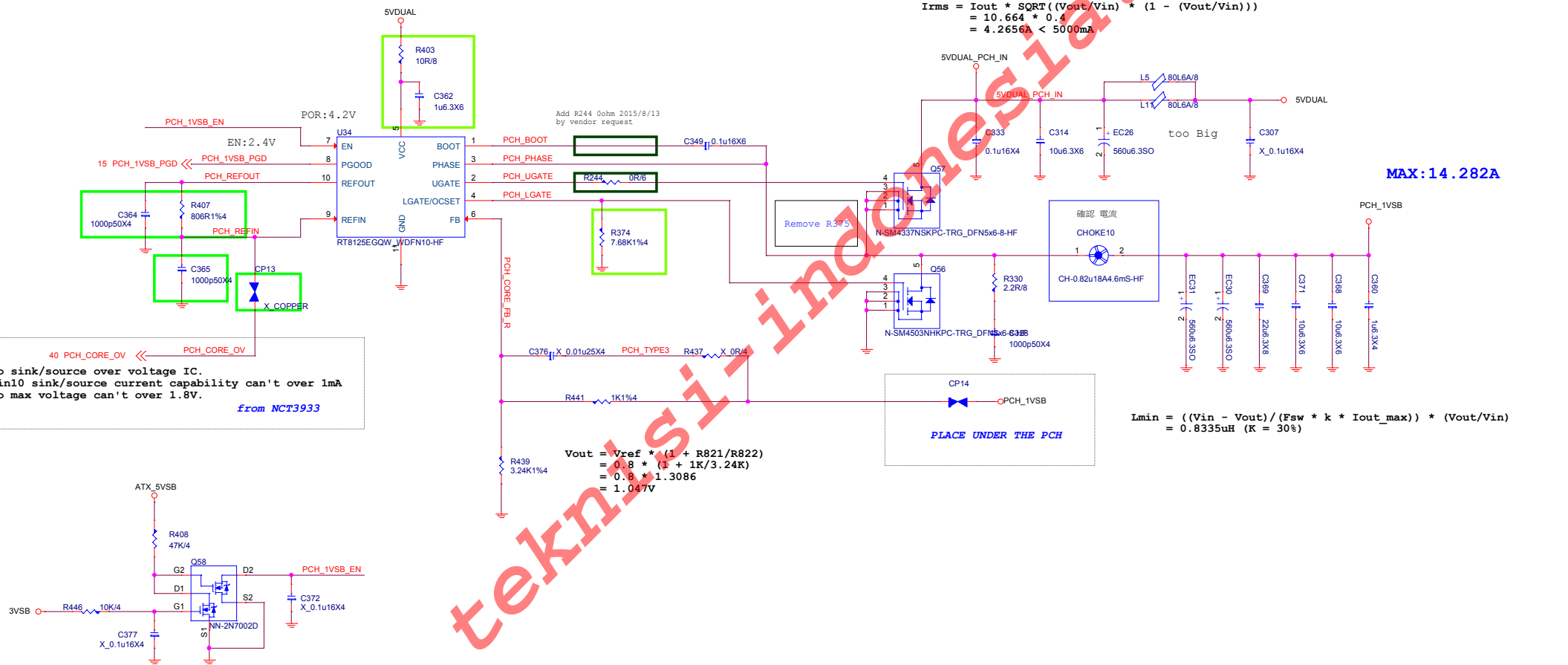
$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.24K)$$

$$= 0.8 * 1.3086$$

$$= 1.047V$$

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Size	Document Description	Rev
Custom	PCH Core power	10
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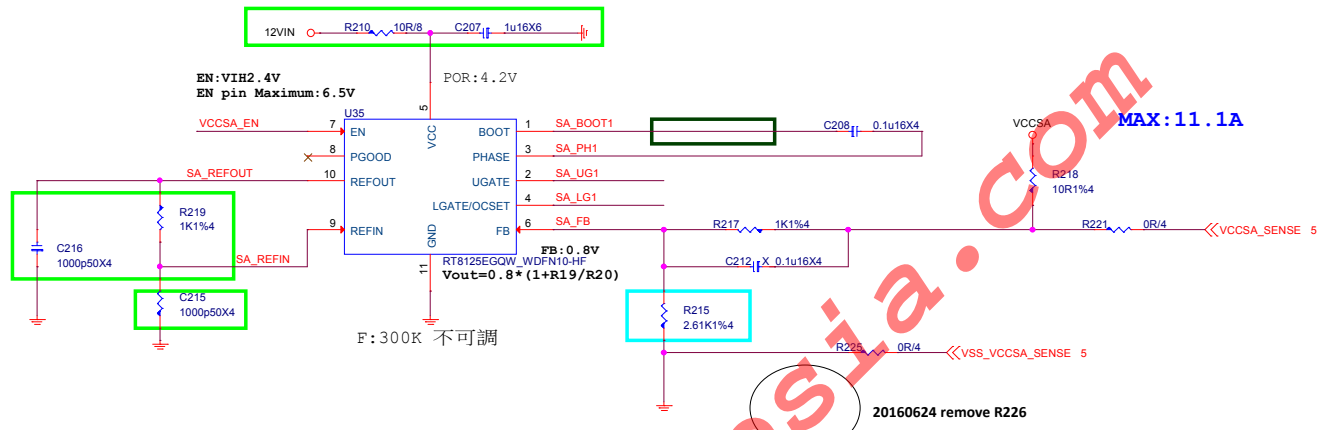
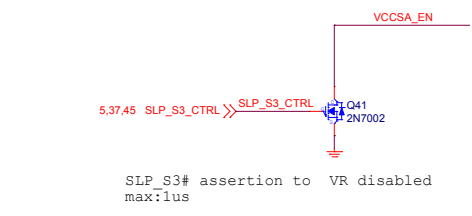
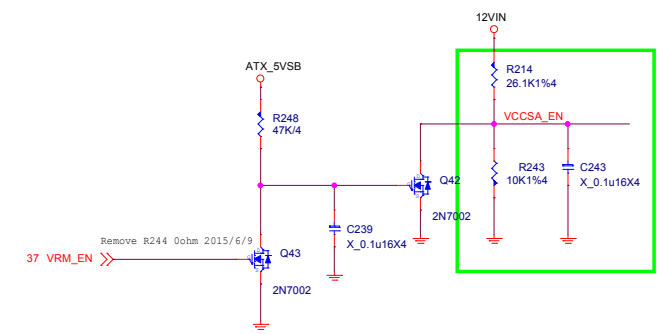
SA Power:1.05V,11.1A

$OCP = 11.1A * 1.84 = 20.44A$
 $R_{ocs}(R15) = OCP * R_{dson}(Low\ side) / 10uA$
 $= 20.44 * (2.5)mohm / 10uA$
 $= 5.11Kohm$

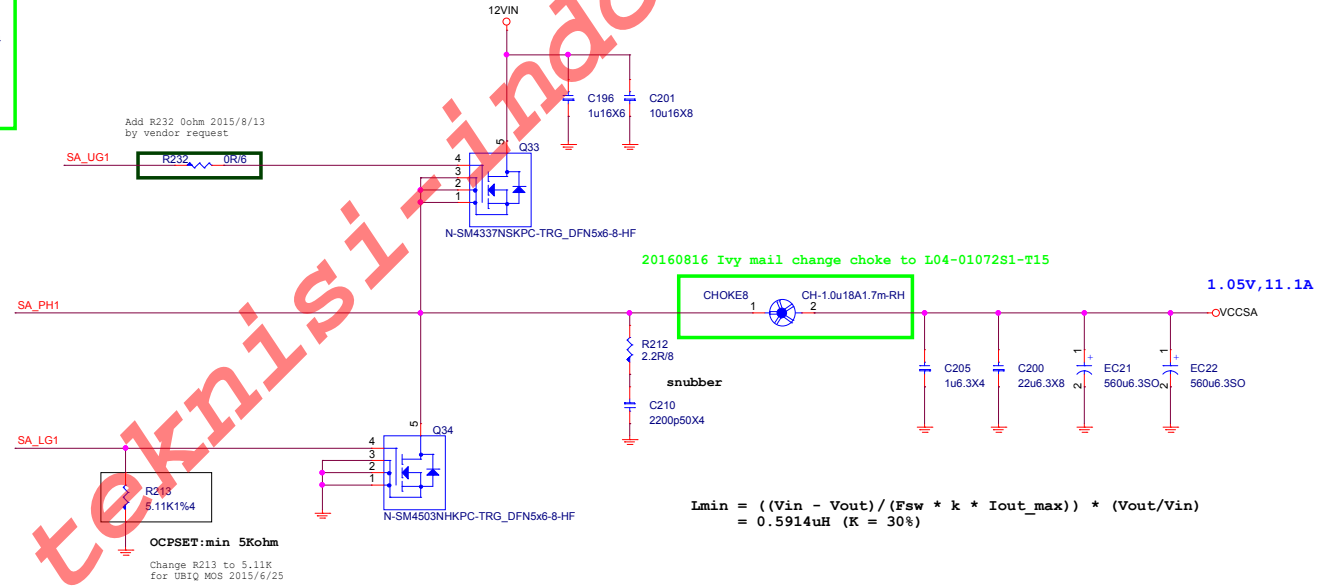
Rocs: 5.2836K, OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A

Rocs: 5.11K
when use UBIQ MOS : 20.44A

Rdson (low) 10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

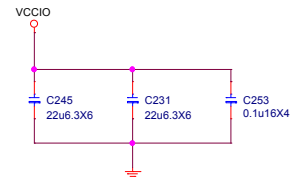


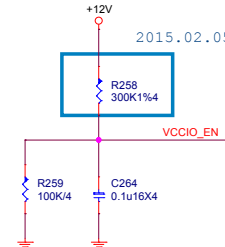
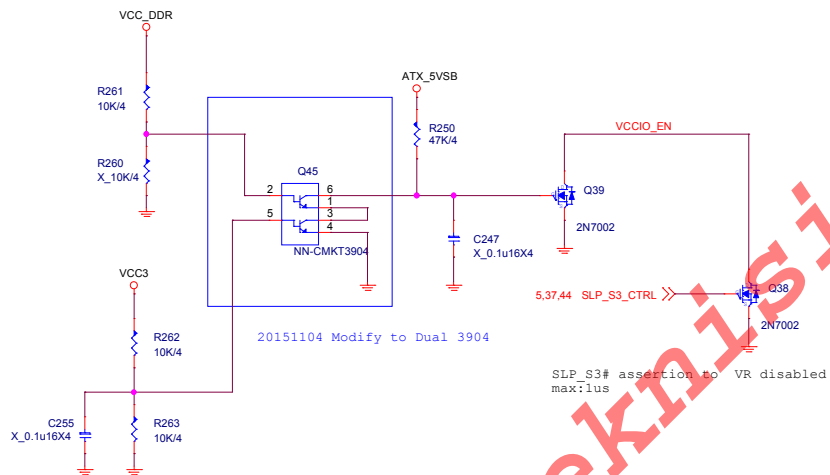
$I_{rms} = I_{out} * \sqrt{((V_{out}/V_{in}) * (1 - (V_{out}/V_{in})))}$
 $= 11.1 * 0.2825$
 $= 3.13575A$



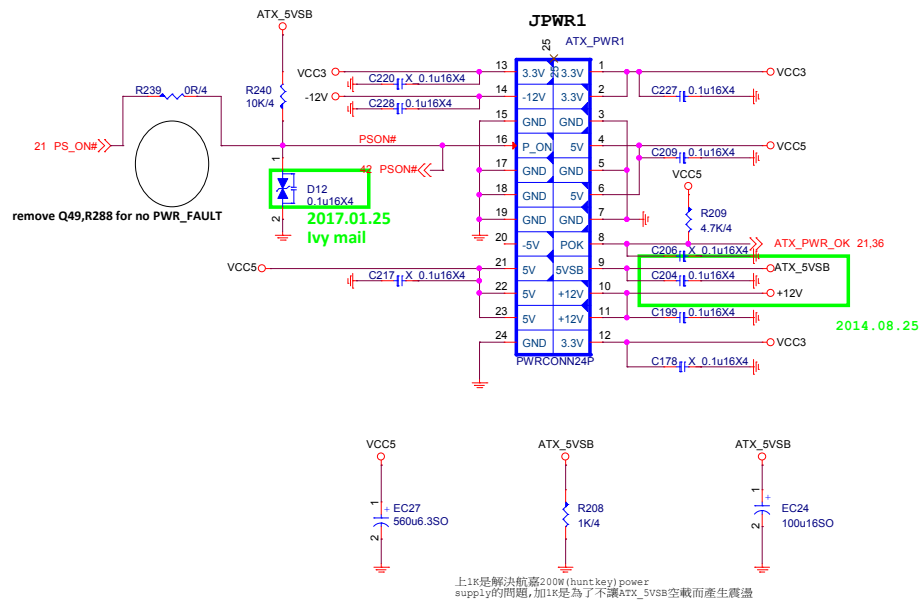
$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$
 $= 0.5914uH (K = 30\%)$

0.95V; 5.5A

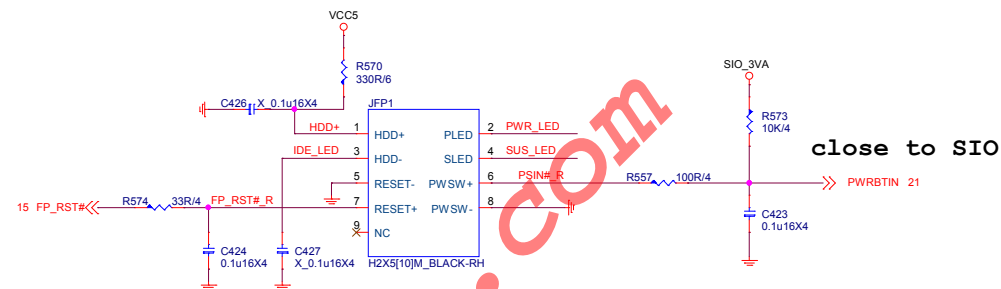

$$T_{ss} = (1/3) * ((V_{out} * C_{ss}) / I_{ss}), I_{ss} = 9\mu A$$

$$T_{ss} = (1/3) * ((1 * 22n) / 9\mu A) = 0.814mS$$


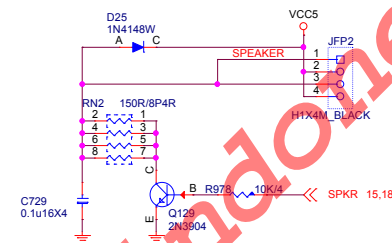
ATX POWER CONNECTOR



FRONT PANNEL



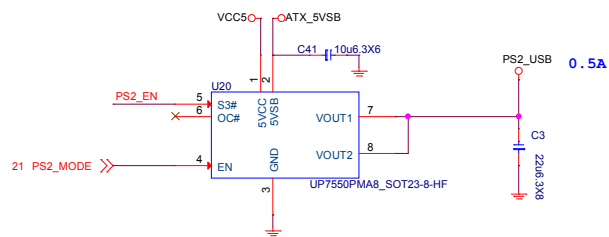
Speaker Pin Header



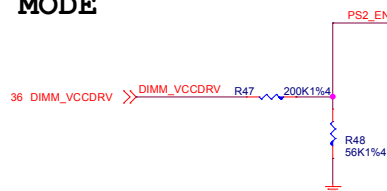
BEEP CIRCUIT

2016.06.02 Ivy mail
remove BEEP Circuit

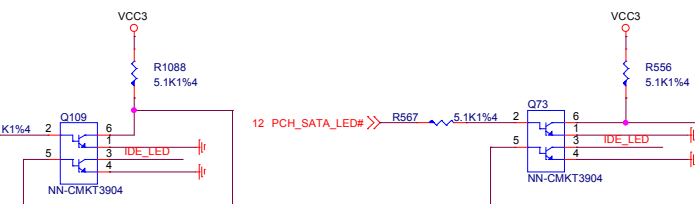
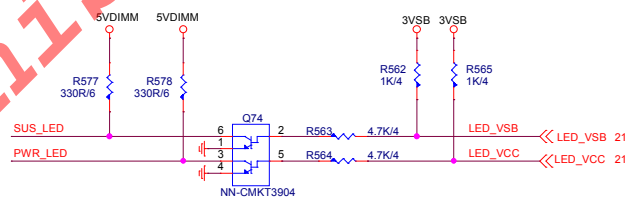
PS2 POWER



USB MODE



LED (for NV5533)



TPM

8/10 remove JTPM1

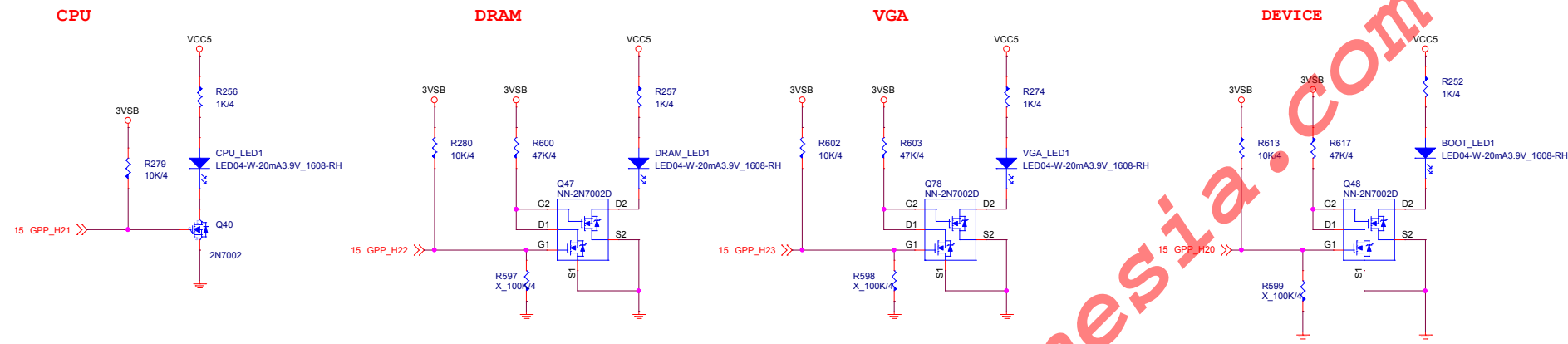


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DEBUG LED

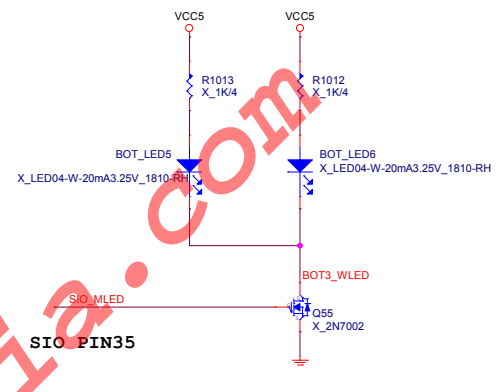
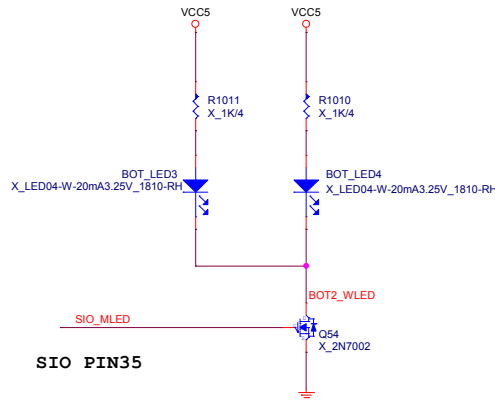
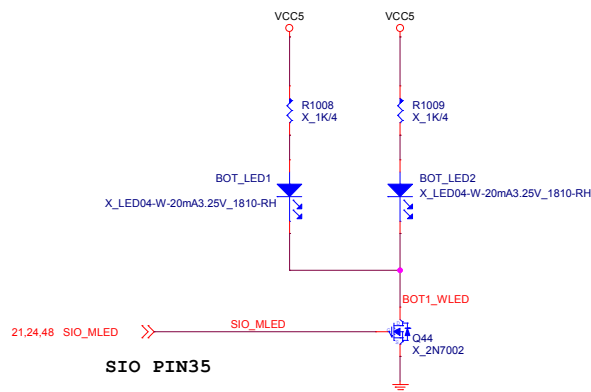


LED \	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

LED
RED:D0C-040P100-H91
AVL:D0C-040S500-E07

WHI:D0C-040T200-H91
AVL:D0C-040S200-E07

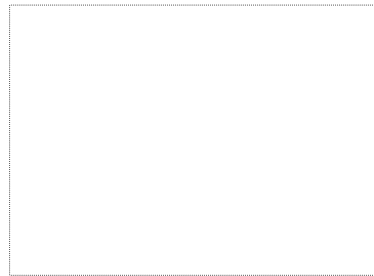
- 開機斷電狀態下，3個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
 2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
 3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
 4. 因此最後正常順利開機後，三個LED燈都是滅掉的。（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）



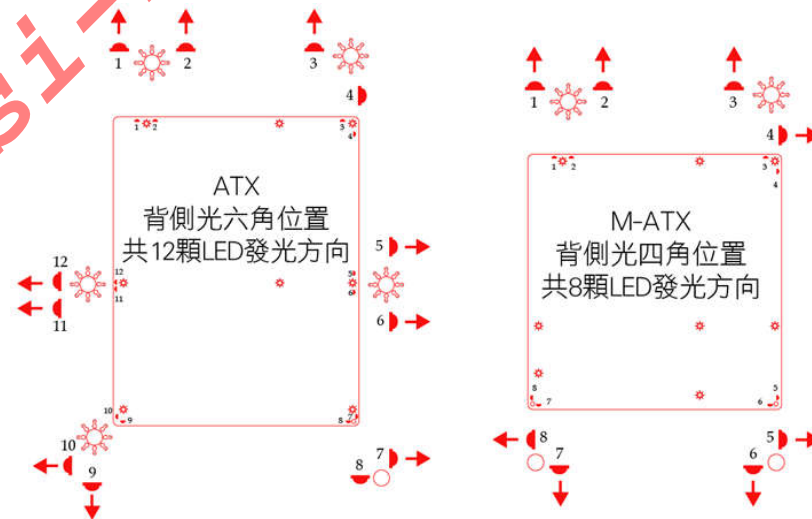
10/11 PM requires to remove ALL BOT LED

LED
紅 : D0C-040S600-E07

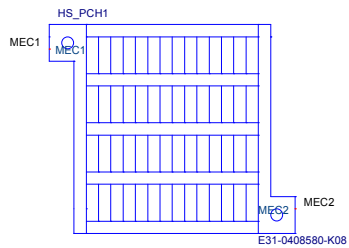
LED
白 : D0C-040T300-H91
AVL: D0C-040S300-E07



0824 remove BOT_LED7 & BOT_LED8

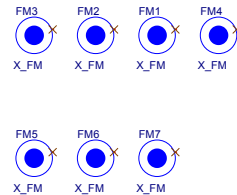


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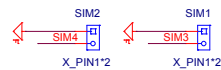


2016.09.23 HS change to E31-0408580-K08

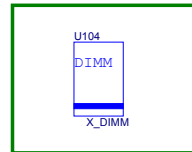
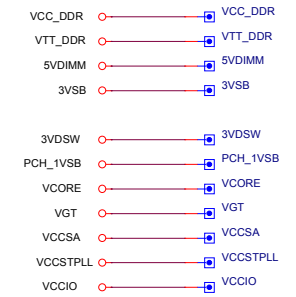
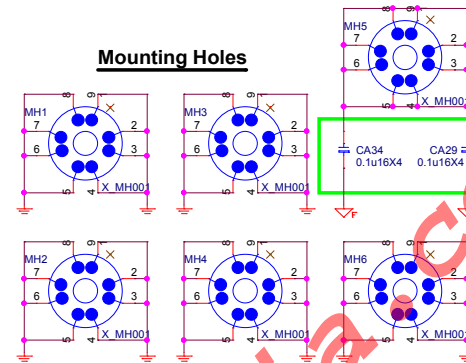
Optical Fiducial Marks-120



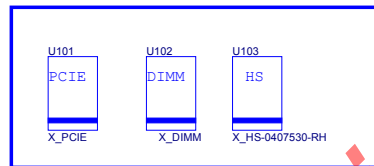
Simulation



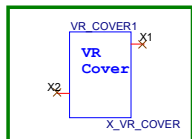
Mounting Holes



2016.11.18 change DIMM for Opt.E/F



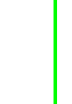
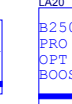
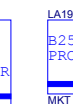
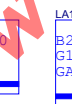
2016.10.26 change PCIE slot + DIMM + HS for B250M G1 GAMER



20160621 PM Request

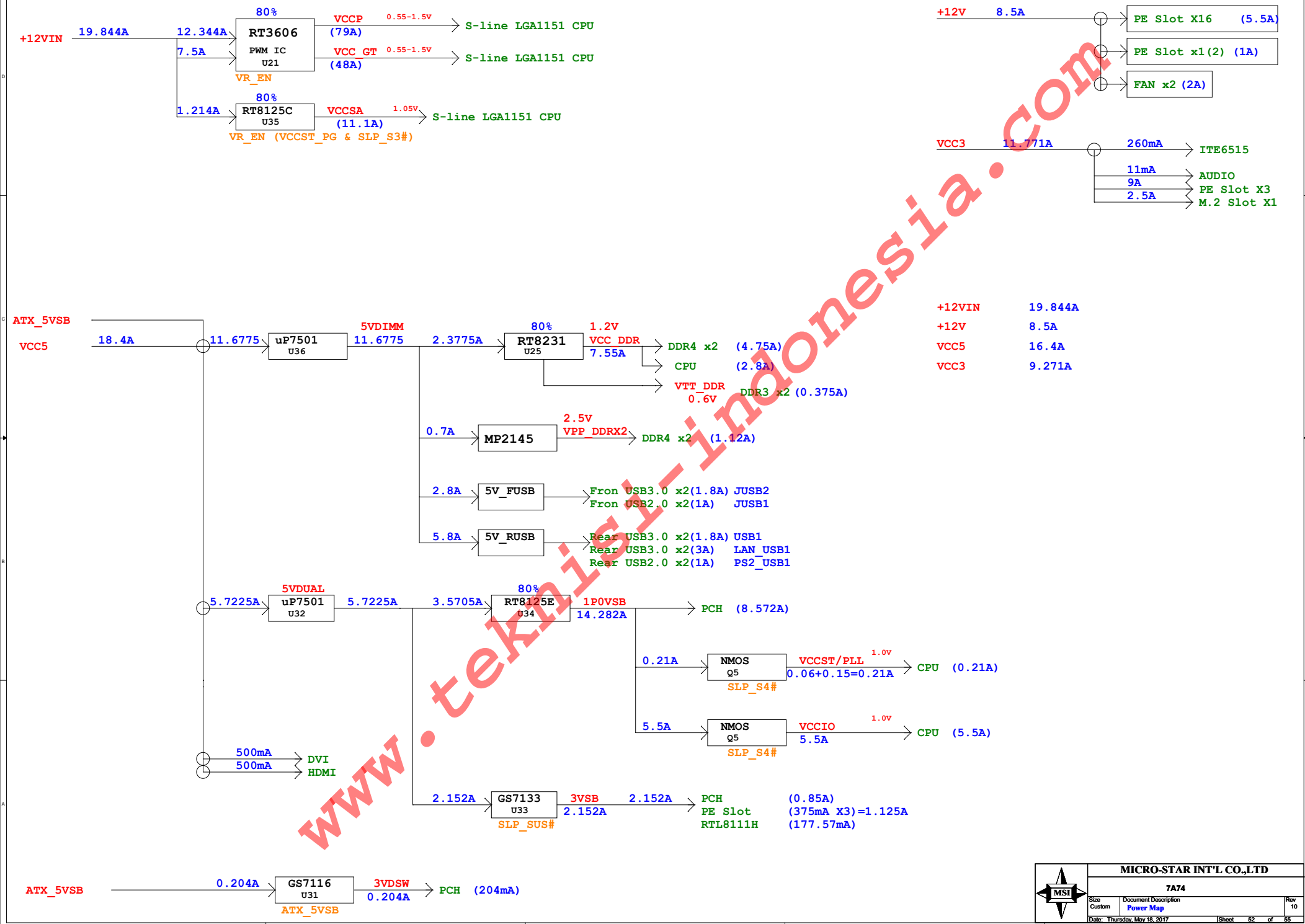


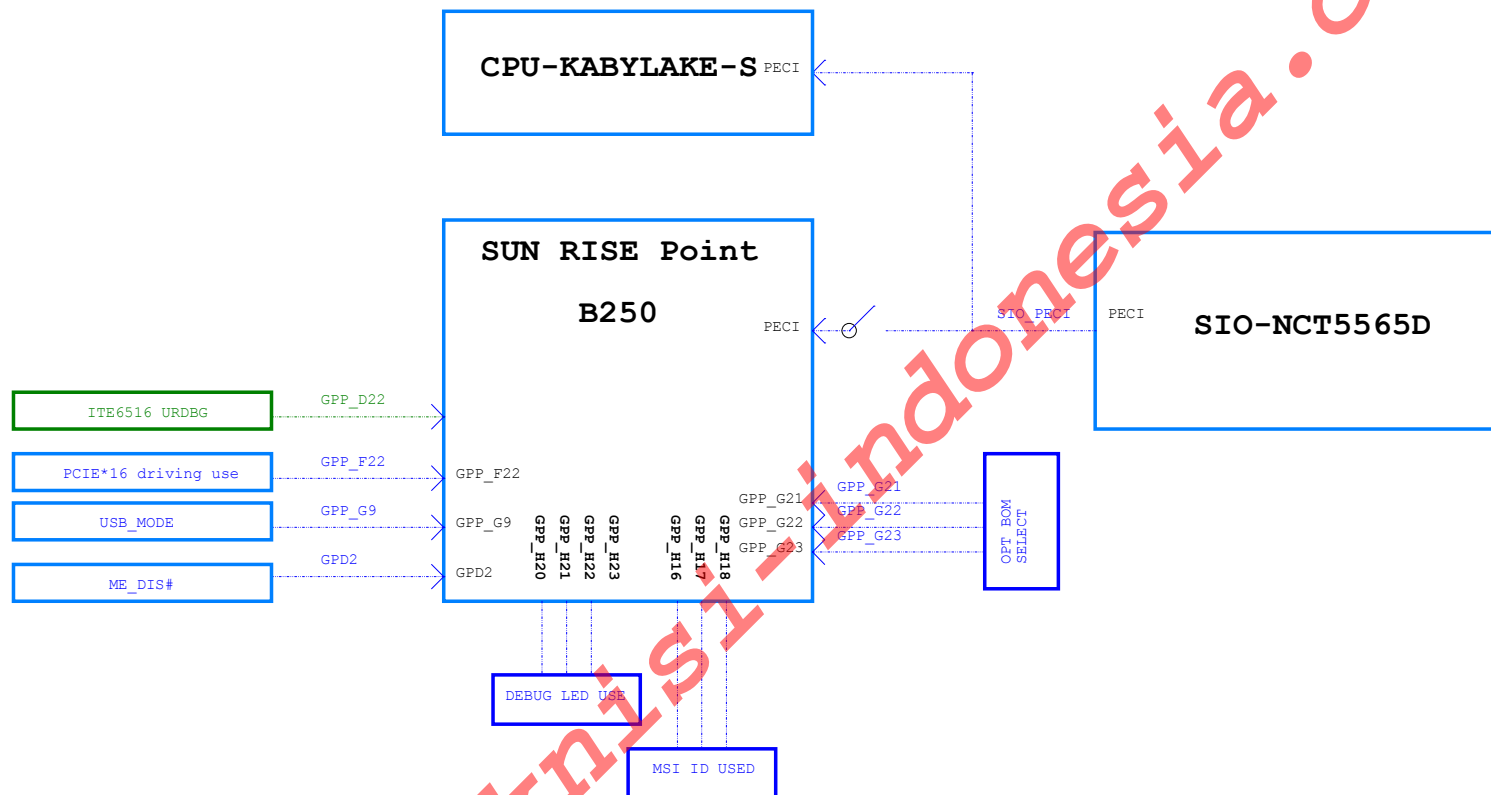
Marketing Name貼紙



PK0-07A7410-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)

Power Delivery





(G3)DS5 ---> S0

VCCRTC (MB-->PCH)

RTCRST# (MB-->PCH)

ATX_5VSB (By PSU)

3VDSW (By ATX_5VSB)

SIO_DPWROK (SIO-->PCH)

SLP_SUS# (PCH-->SIO)

SYS3VSB_OFF (By BJT)

3VSB (By SIO)

5VDUAL (By SIO)

PCH_1VSB (By 3VSB)

RSMRST# (By SIO to PCH)

PWRBTN# (to SIO to PCH) (CP Internal 16ms debounce)

SLP_S5# (By PCH to ???)

SLP_S4# (By PCH to SIO)

SLP_S3# (By PCH to SIO)

PSON# (By SIO to PS)

VCCSTPLL (By SLP_S4#)

12V/5V/3V (By PSU to MB)

ATX_PWR_OK (By PSU to MB)

5VDIMM (By S3 & S4 & ATX_PWR_OK)

VPP25 (By S4 & 5VDIMM)

VCC_DDR (By VPP25)

VTT_DDR (By VCC_DDR)

VCCIO (By SLP_S3# & VCC_DDR)

IMVP8_EN (By SLP_S3 & VCCIO_PG)

VCCSA (By SLP_S3 & VCCIO)

VRM_PG (By VCCSA)

VCCST_PWRGD (By VRM_PG to CPU)

PCH_PWROK (By VRM_PG to PCH)

PCH_CLKOUT (By PCH_PWROK)

CHIP_PWGD (By SIO to PCH)

CPU_PWRGD (By PCH_PWROK (PCH to CPU))

PLTRST# (By PCH to SIO)

SVID (By VCCST) (Pull up with VCCSTPLL)

VCORE (By SVID)

VGT (By SVID)

DRAM_RESET# (By PCH_PWROK)

S0 --> S5

PLTRST# (By SIO to PCH)

CPU_PWRGD (By PCH to CPU)

PCH_CLKOUT (By PCH)

SLP_S3# (By PCH to SIO)

CHIP_PWGD (By SIO to PCH)

VRM_EN (By S3# Reverse)

VCCIO_EN

VRM_PG

VCCST_PWRGD

PCH_PWROK (By VRM_CORE_PG)

VCCIO

VCORE

VCCSA

PSON# (By SIO to PS)

ATX_PWR_OK (By PSU)

12V/5V/3V

SLP_S4# (By PCH to SIO)

DRAM_RESET# (By PCH to DIMM)

VCC_DDR

VPP25

THERMTRIP#

SVID

VCCSTPLL

SLP_S5# (By PCH to ???)

S5 --> D85

SLP_SUS# (By PCH to SIO)

SIO_SLP_SUS (by SIO to PCH)

3VSB (PCH_1VSB)

RSMRST# (by SIO to PCH)

D85 --> G3

ATX_5VSB

3VDSW

PCH_DPWROK (by SIO to PCH)



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